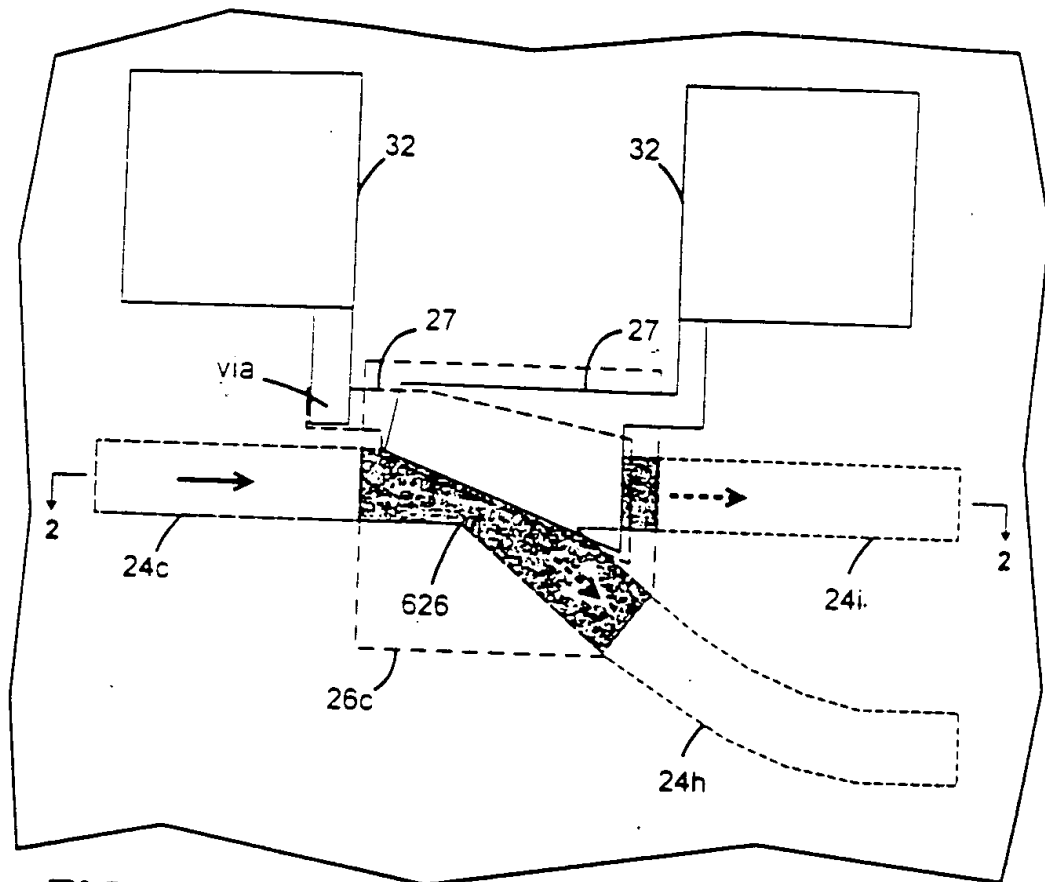


**FIG.\_2**



**FIG. 3**



28c'

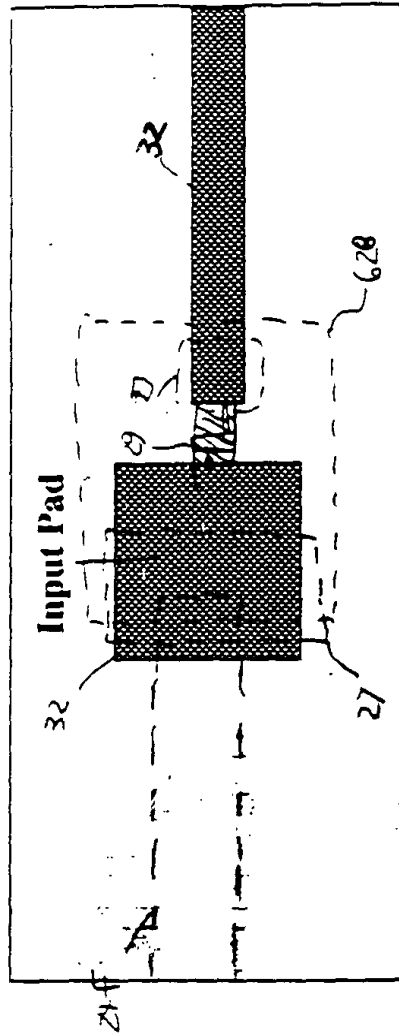


FIG. 5-2

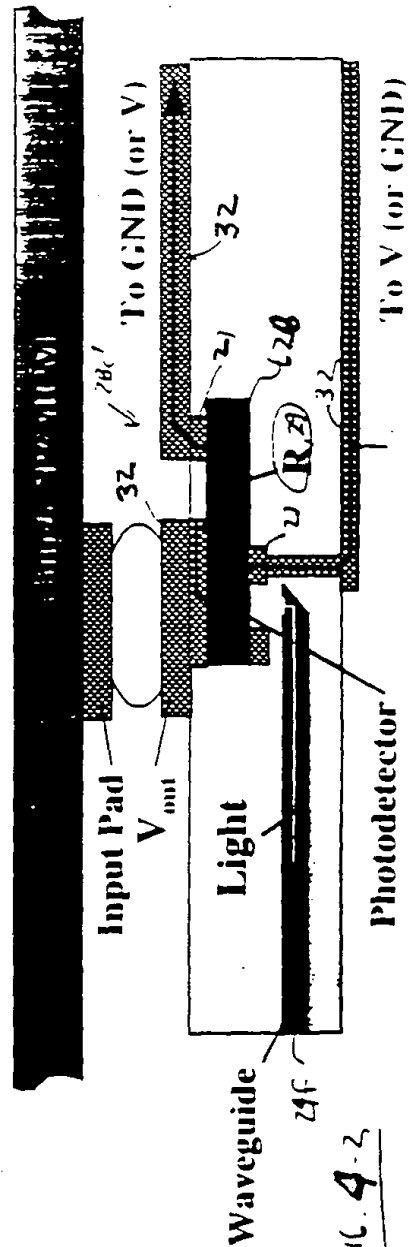


FIG. 4-2

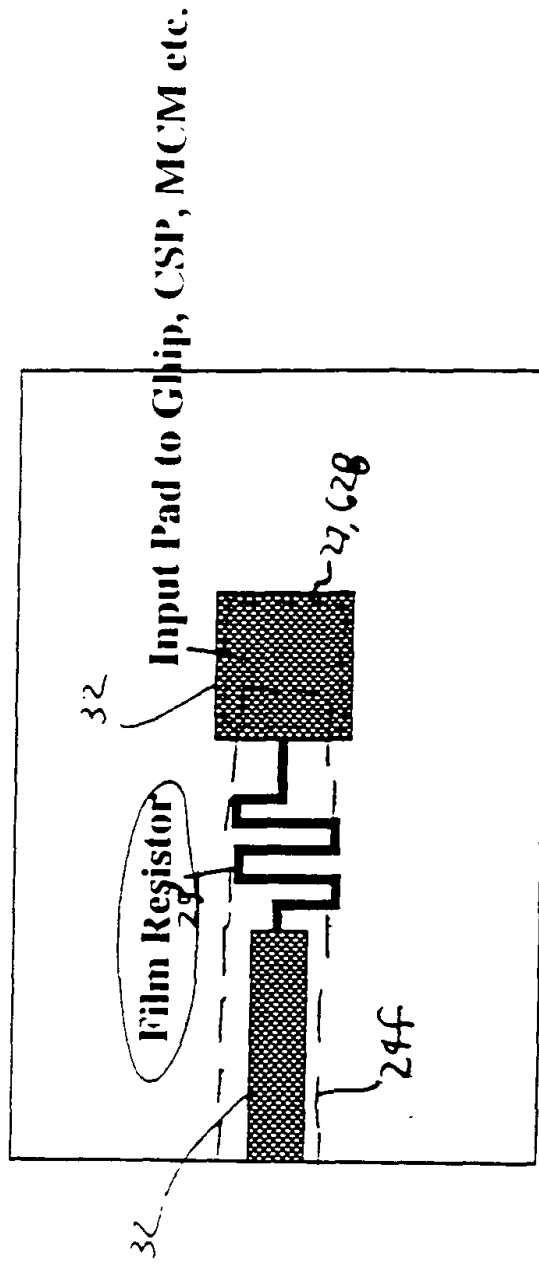


Fig. 5-3

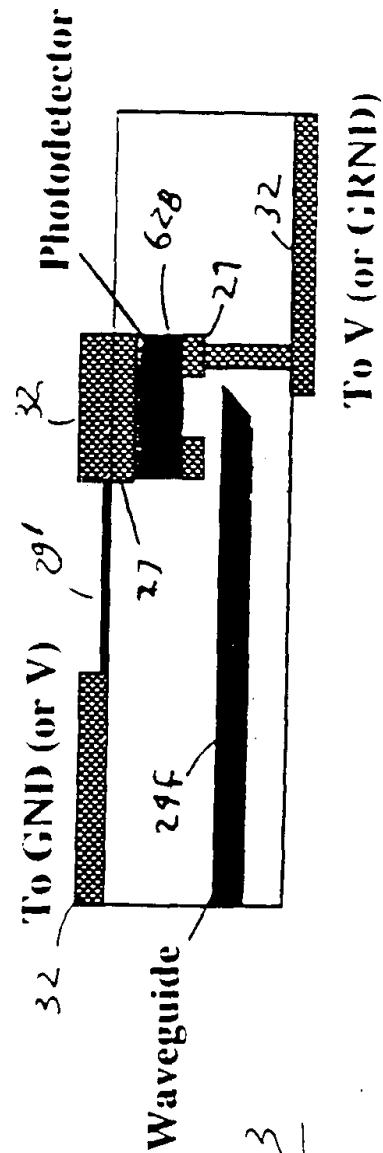


Fig. 4-3

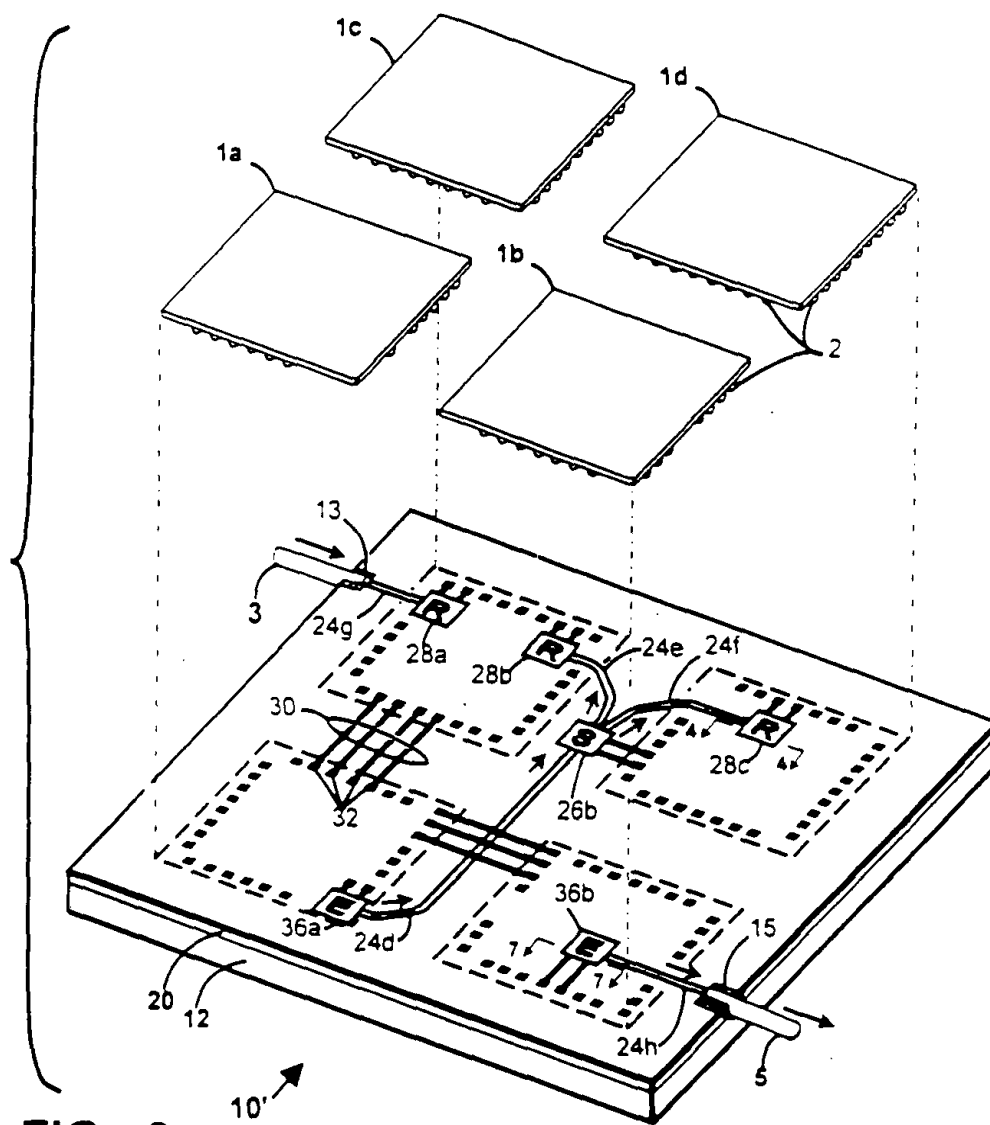


FIG.\_6

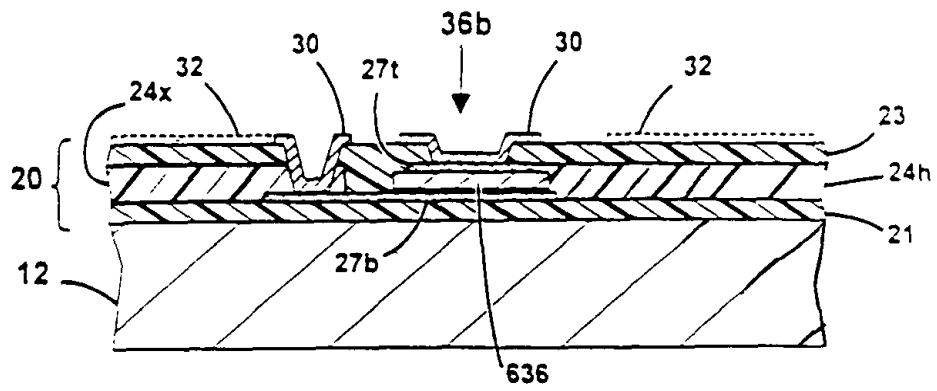


FIG.\_7

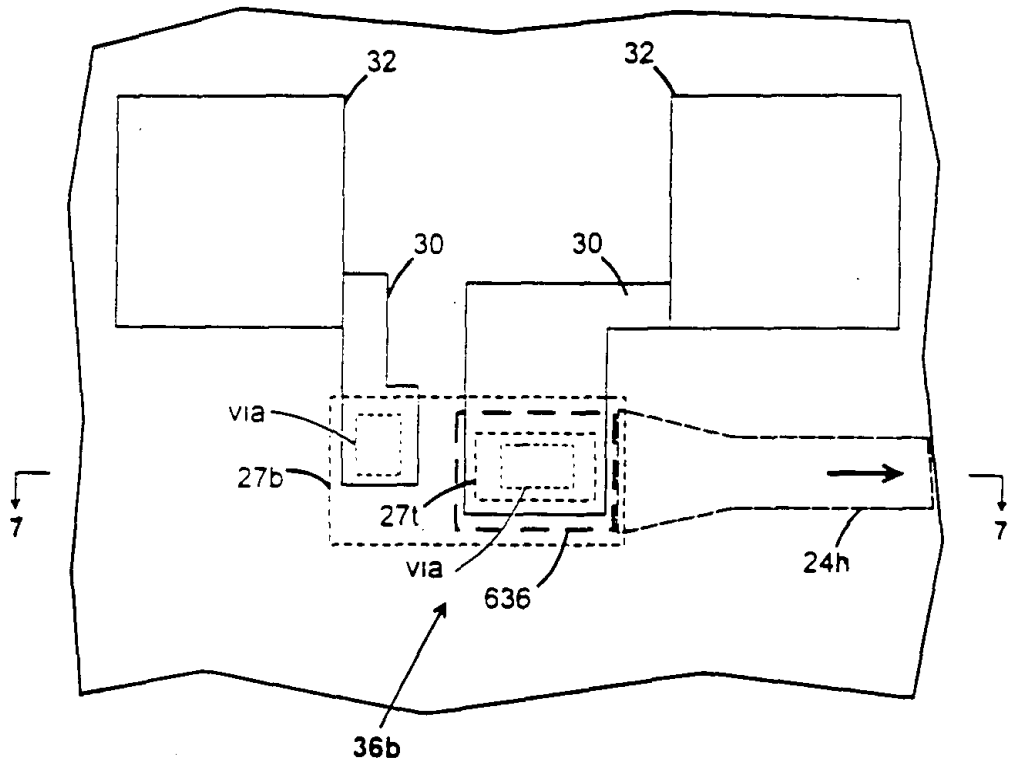
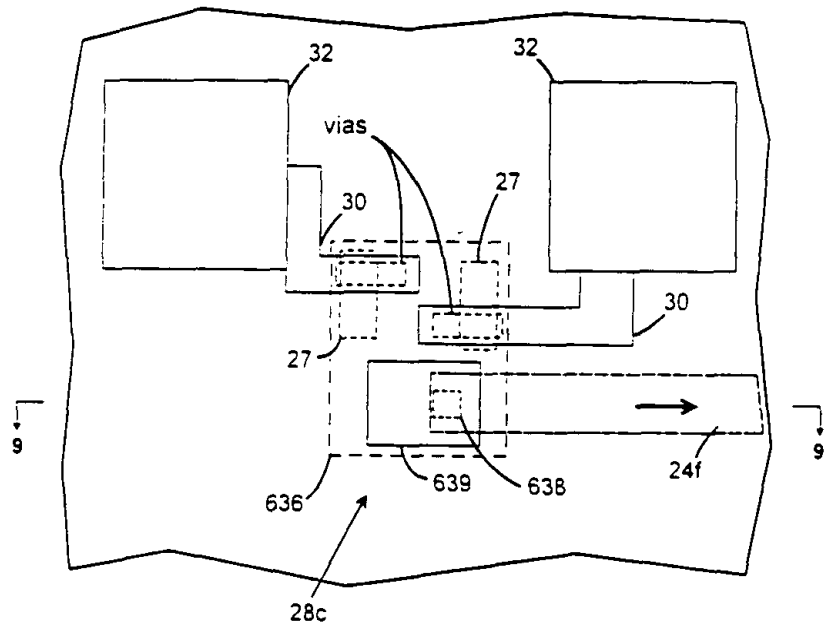
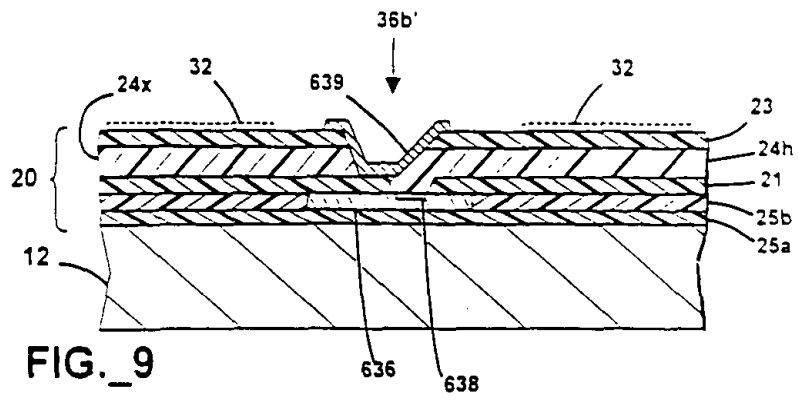


FIG.\_8





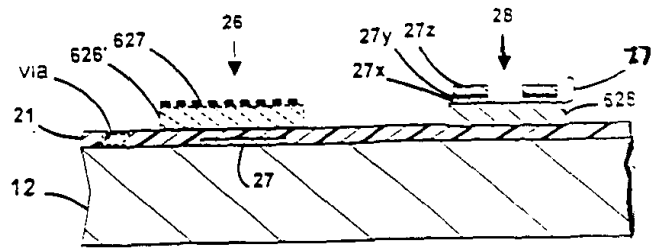


FIG. 11

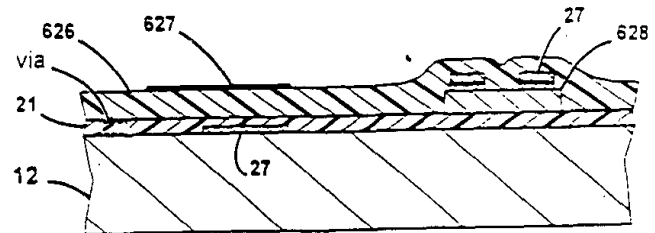


FIG. 12

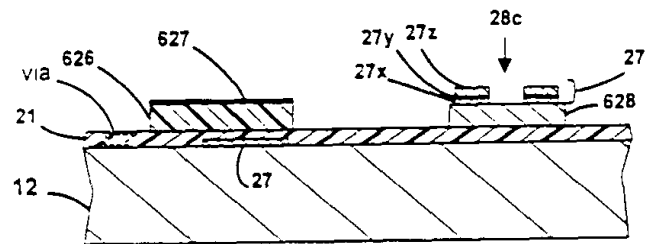


FIG. 13

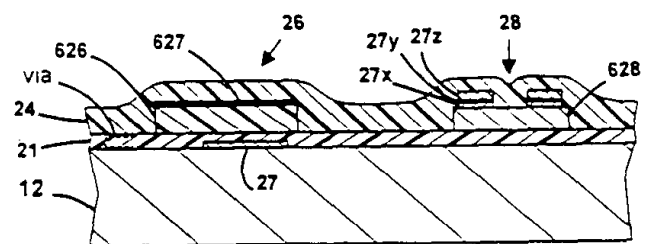


FIG. 14

FIG.\_15

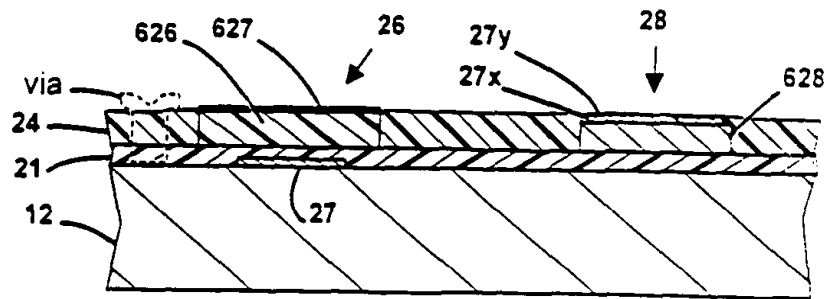


FIG.\_16

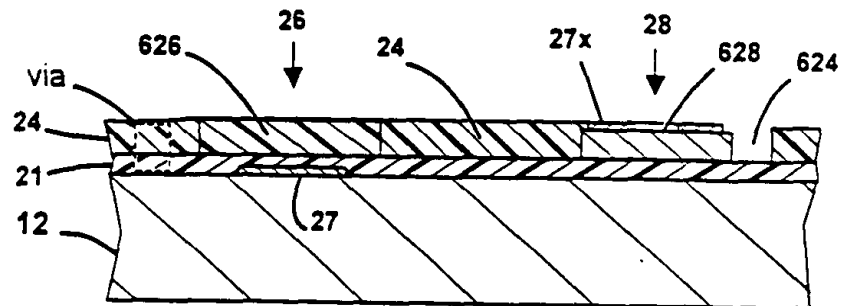


FIG.\_17

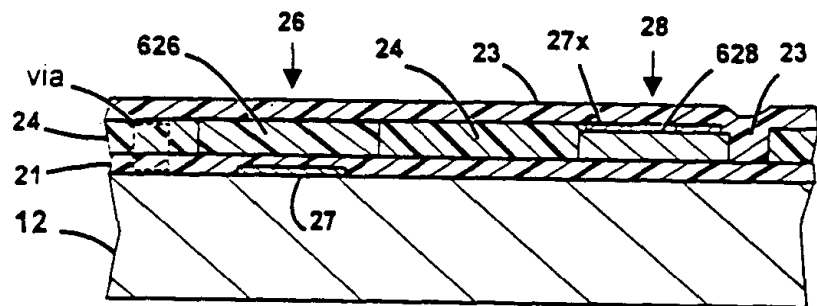
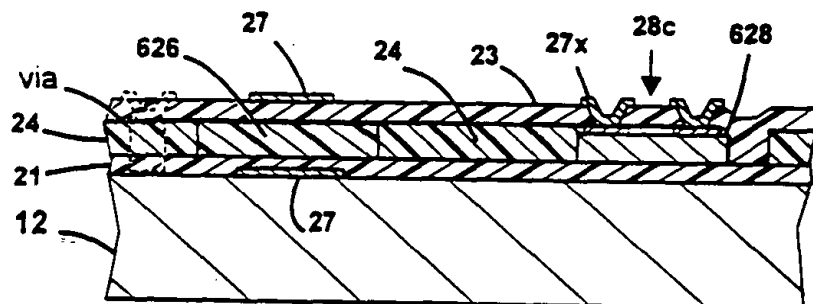


FIG.\_18



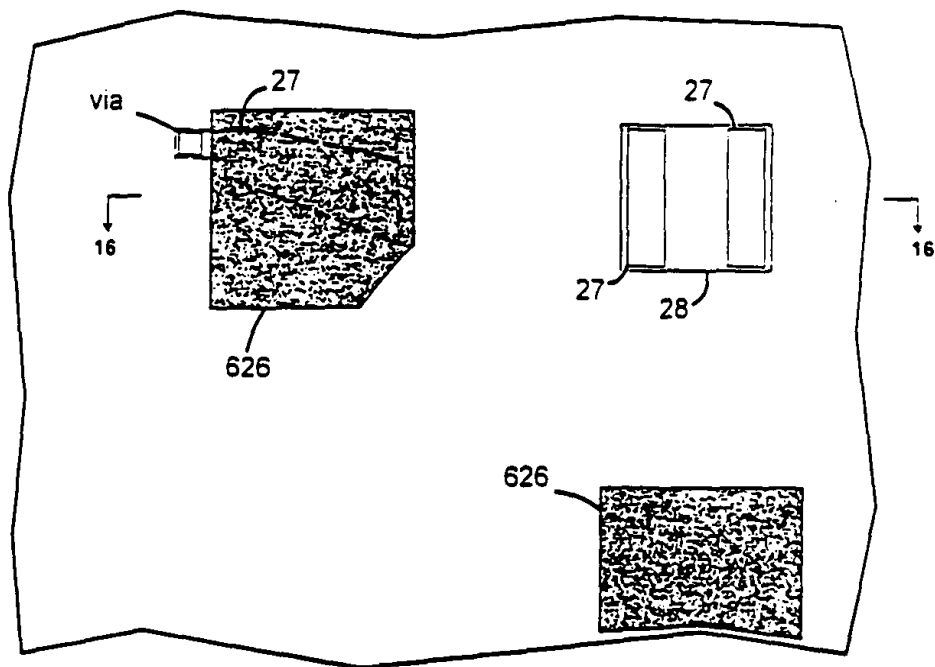


FIG.\_19

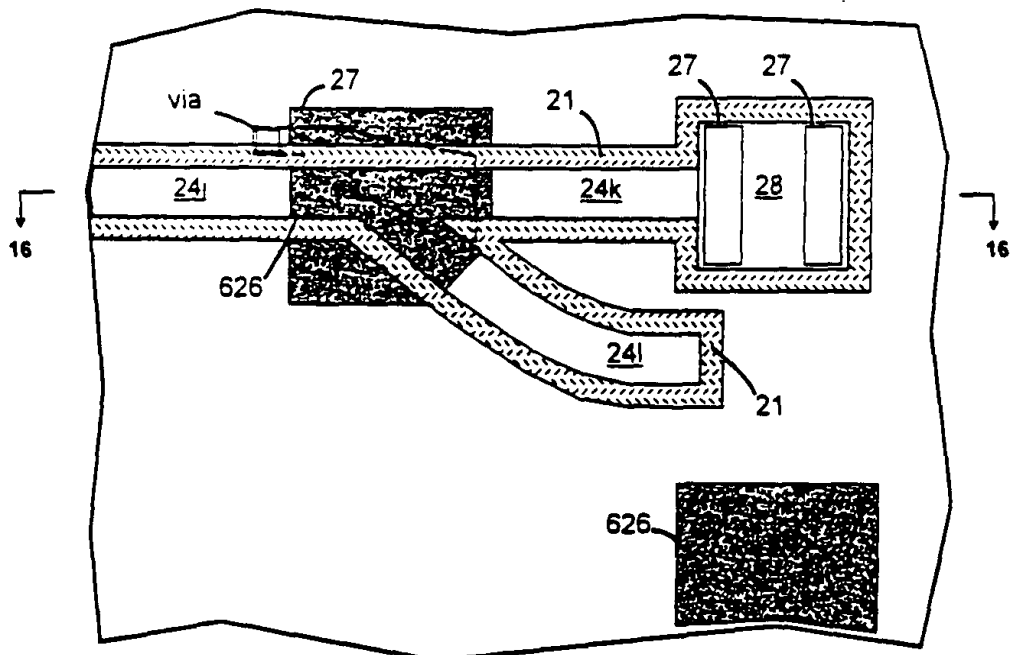
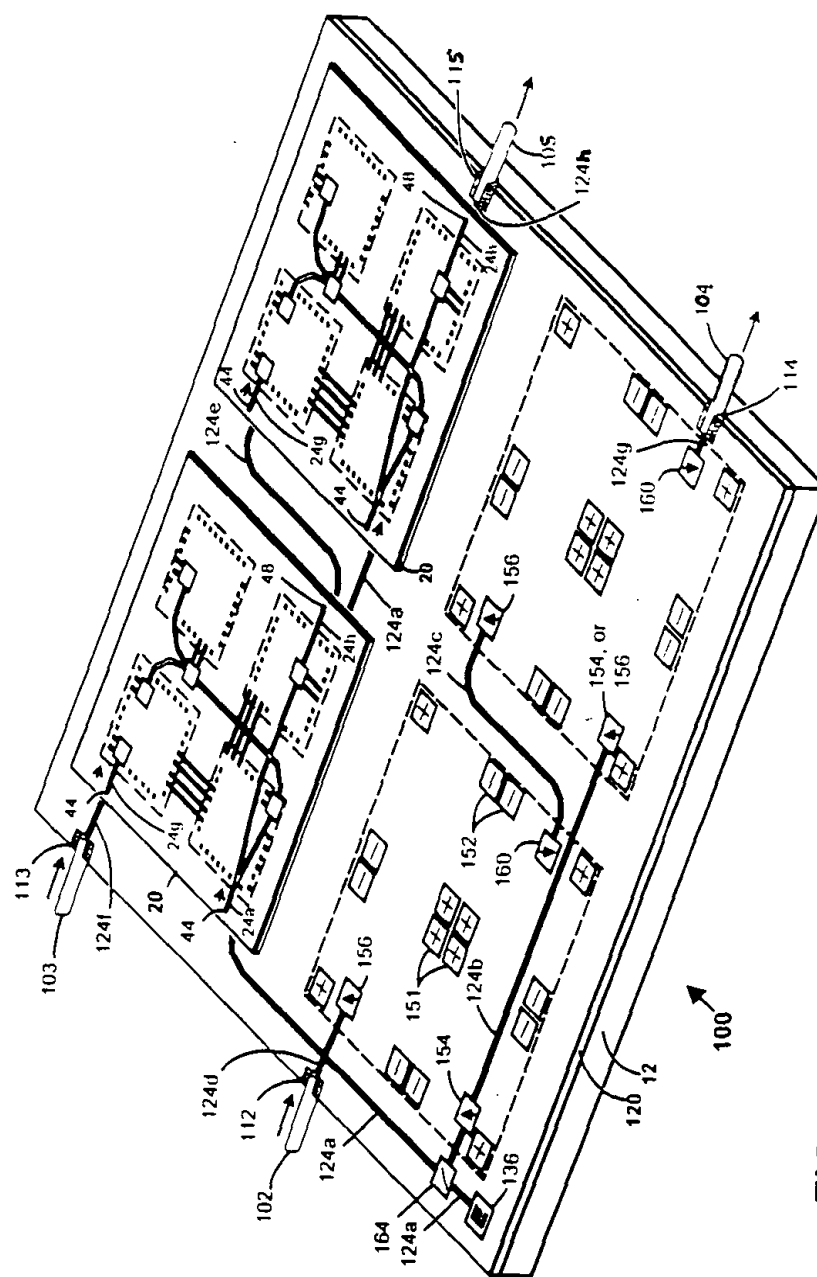
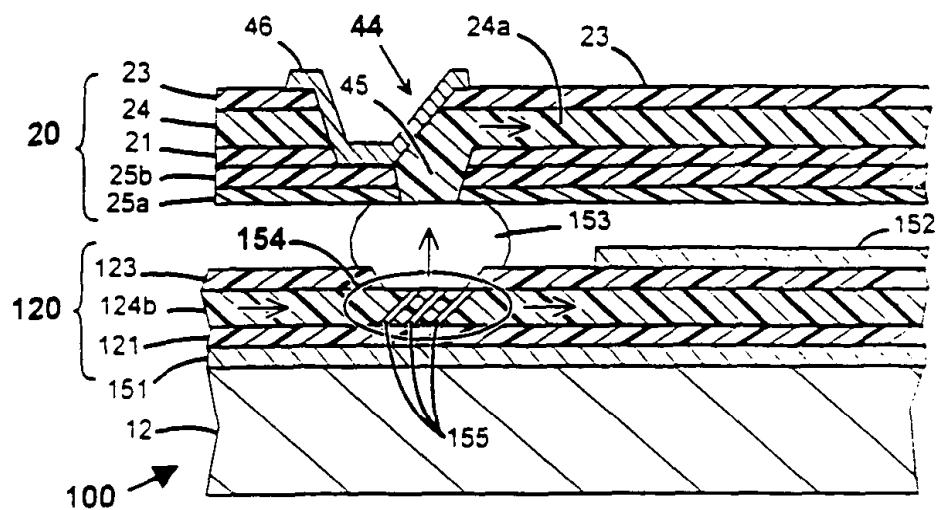


FIG.\_20

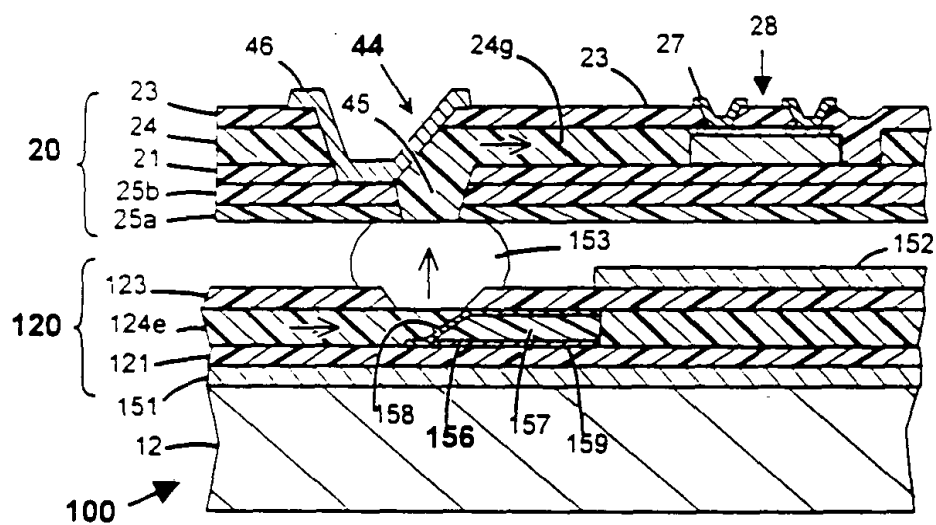
Figure 1: Schematic representation of the 12 genes and their organization in the 120 kb genomic region. The diagram shows 12 genes (A12 to A1) as boxes with arrows indicating their orientation. A scale bar at the bottom indicates 10 kb. The genes are arranged in a cluster, with A12 at the top and A1 at the bottom. The orientation of the genes is indicated by arrows: A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, and A1. The scale bar shows 10 kb increments.



**FIG. 21**

[illegible]

**FIG.\_22**



**FIG.\_23**

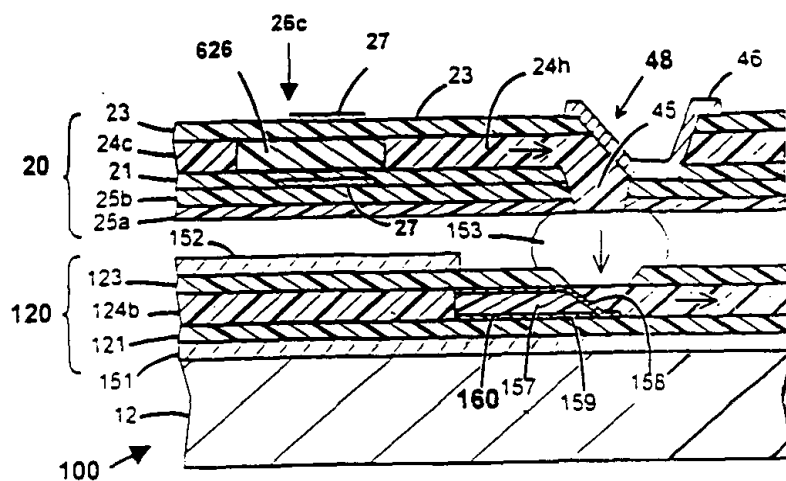


FIG.\_24

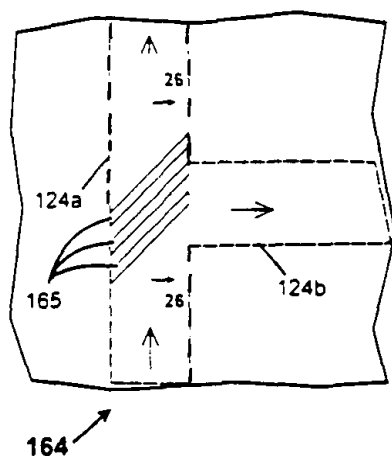


FIG. 25

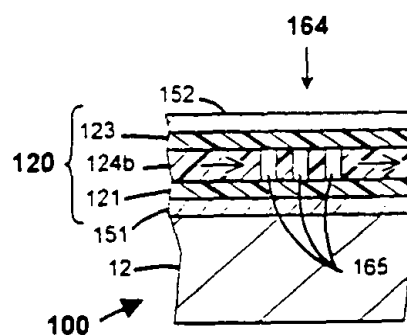


FIG.\_26

FIG.\_27

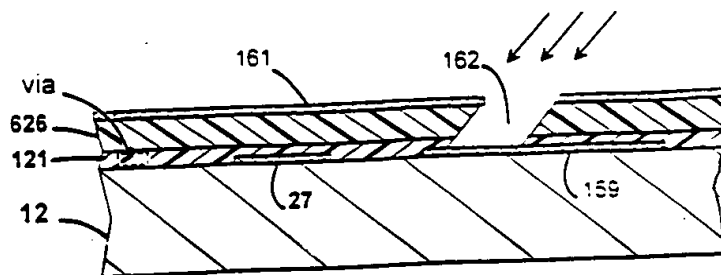


FIG.\_28

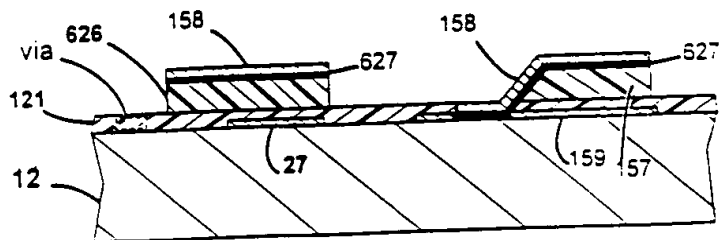


FIG.\_29

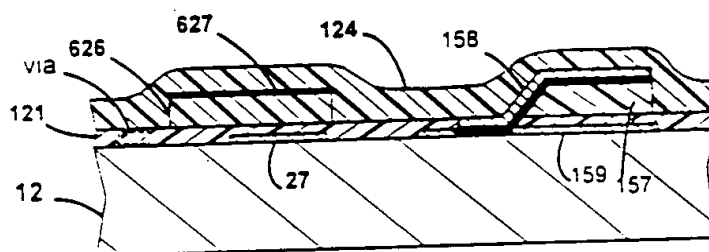
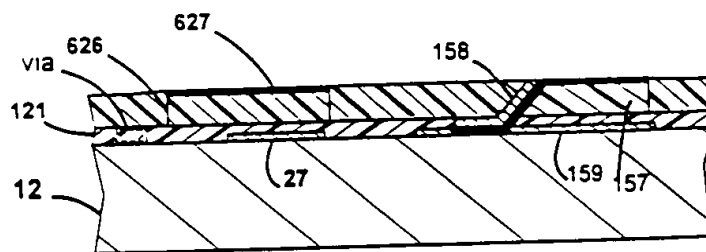


FIG.\_30







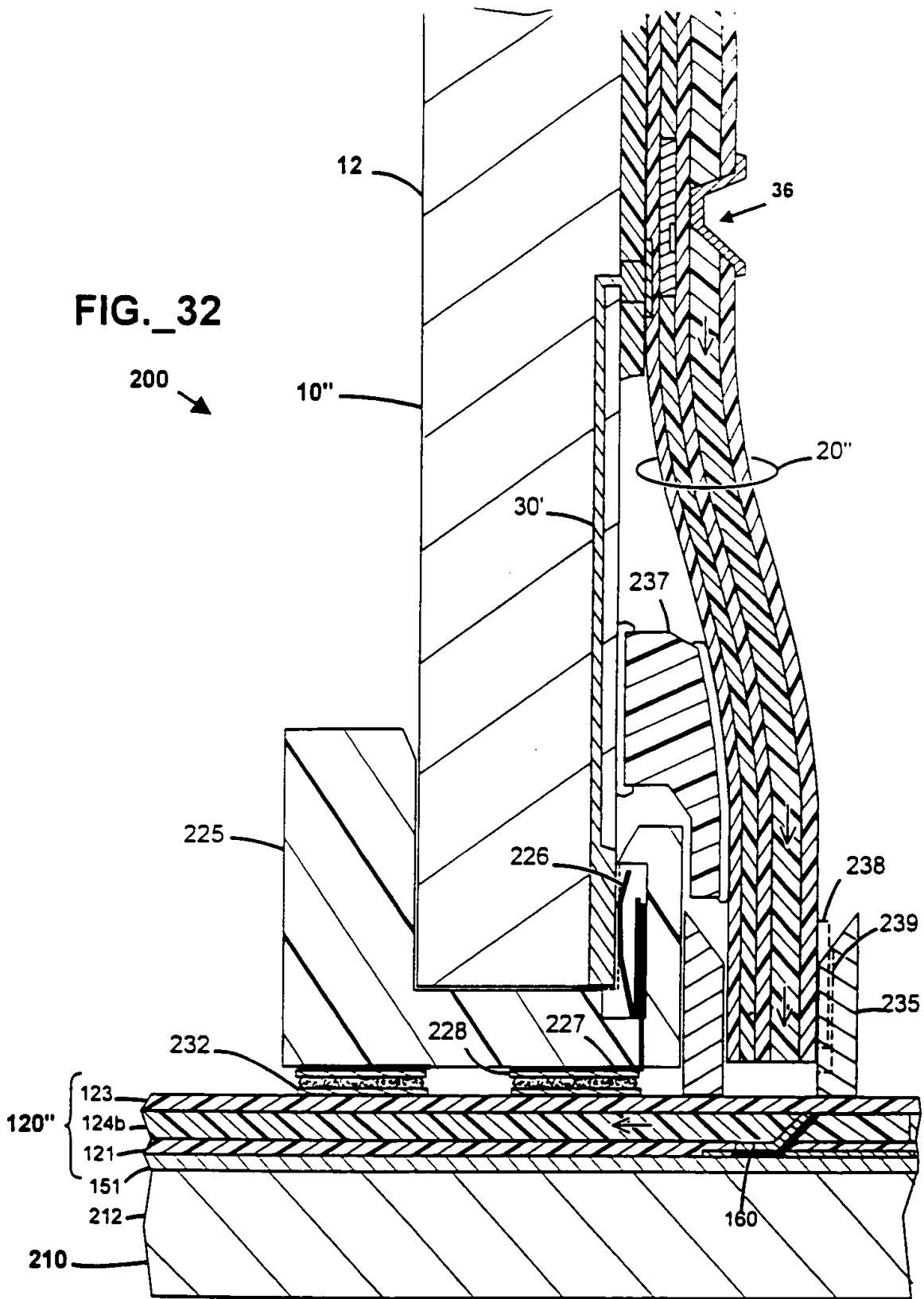
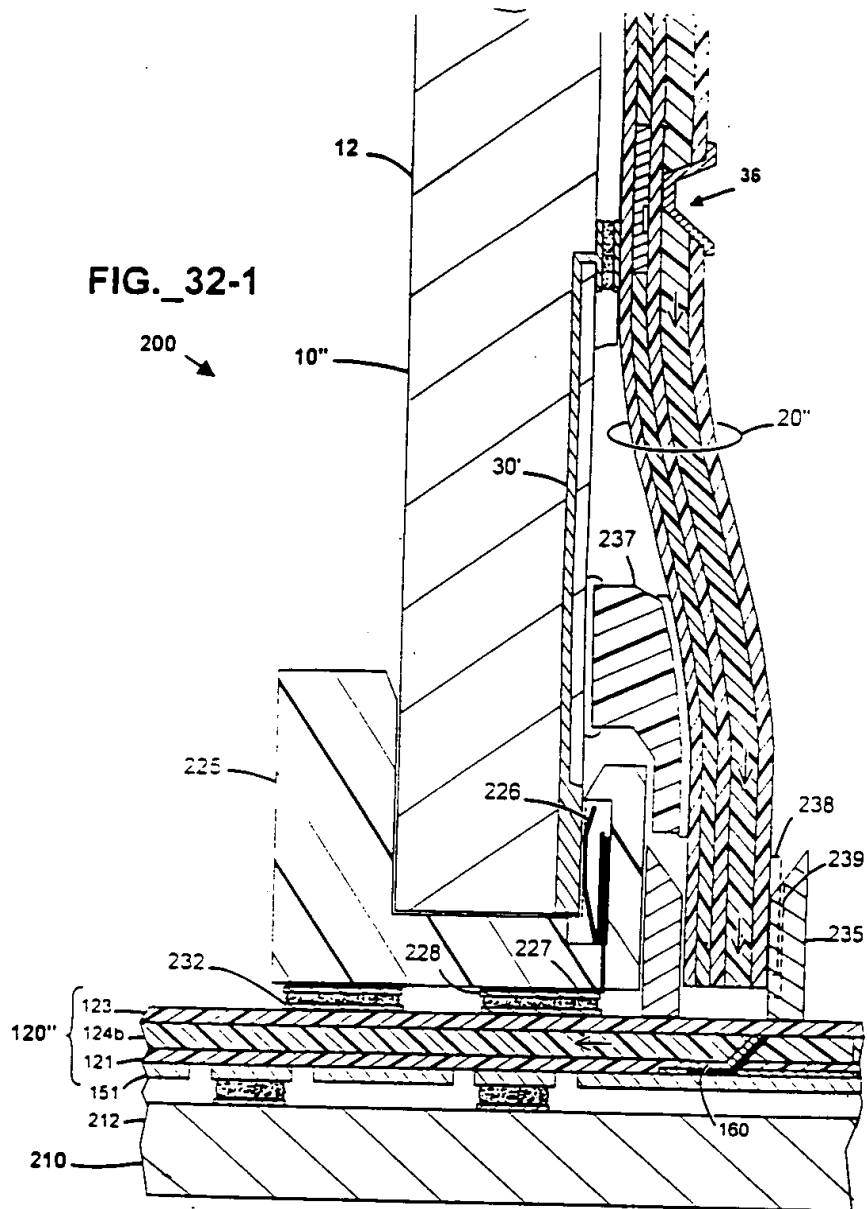
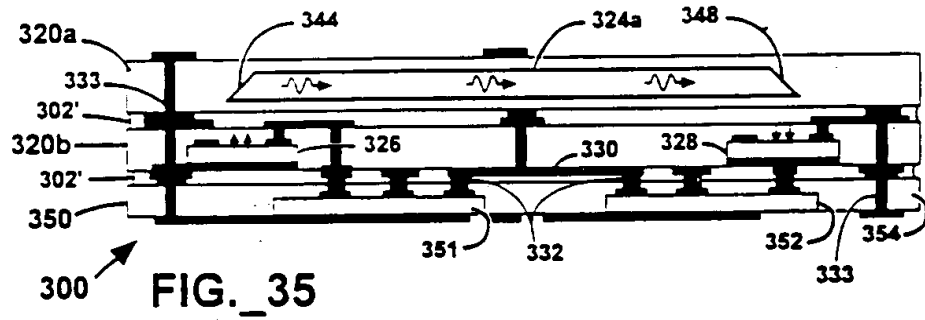
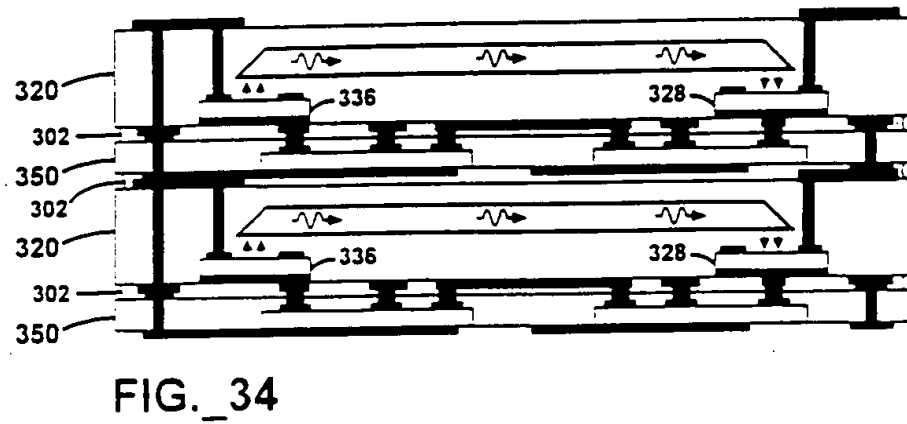
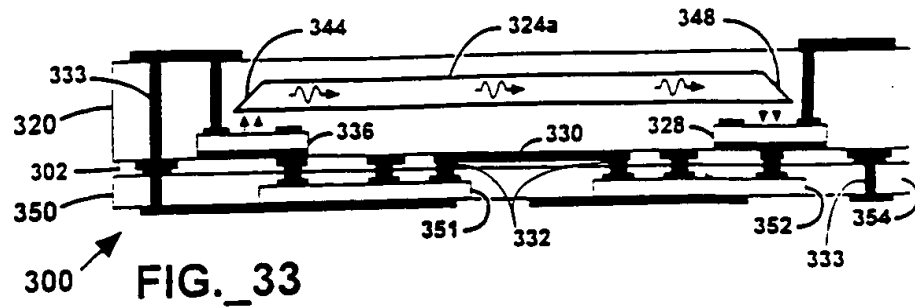


FIG. 32-1





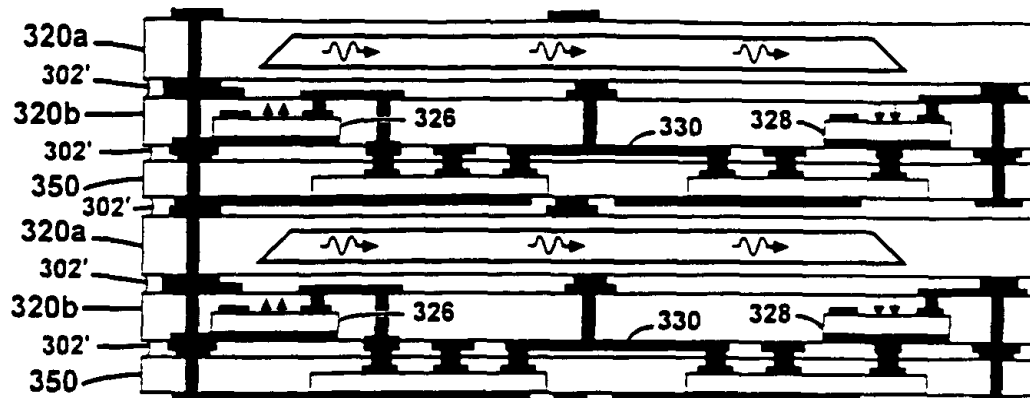


FIG.\_36

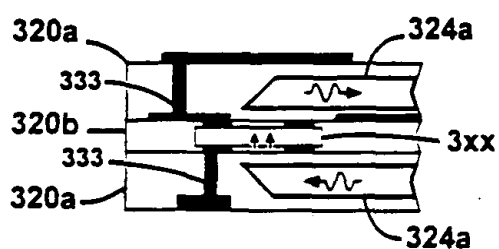


FIG.\_37-1

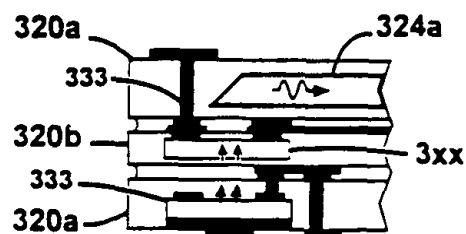


FIG.\_37-2



FIG.\_37-3

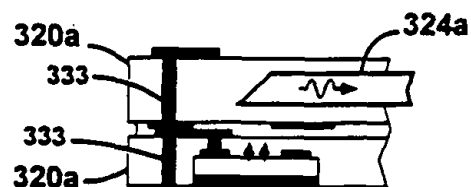


FIG.\_37-4

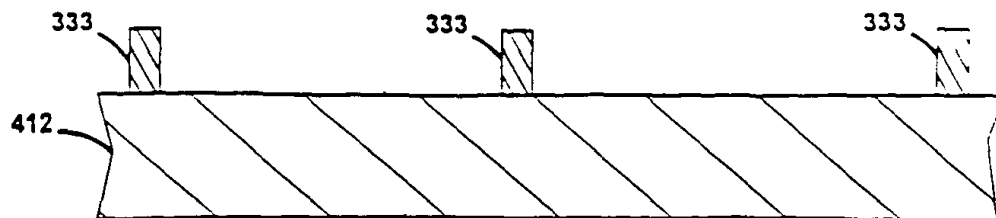


FIG.\_38

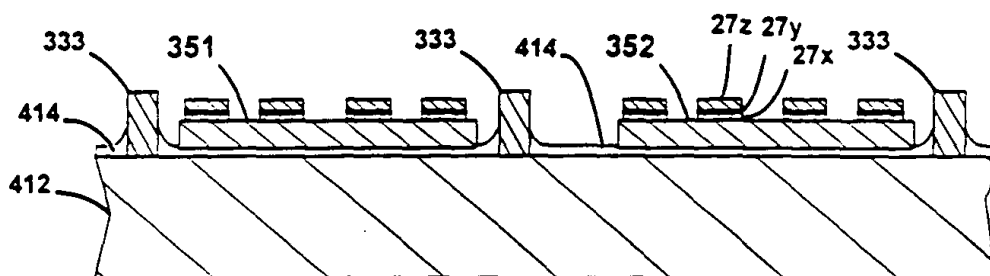


FIG.\_39

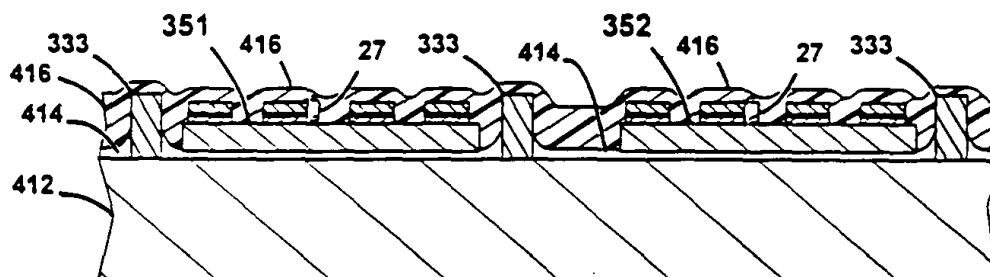


FIG.\_40

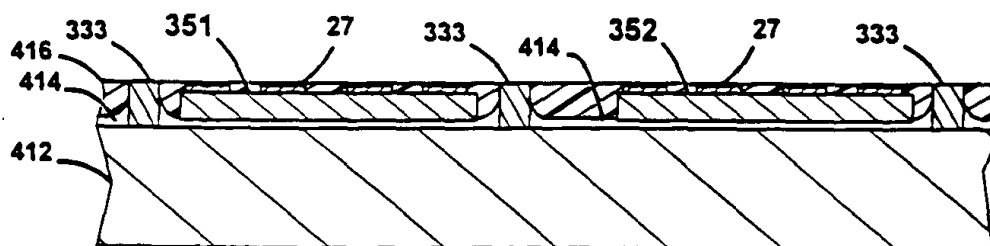


FIG.\_41

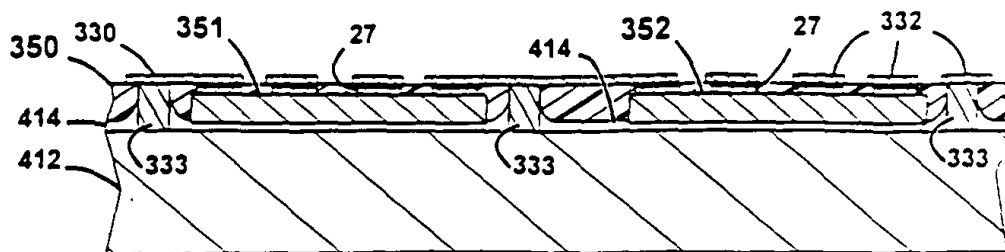


FIG.\_42

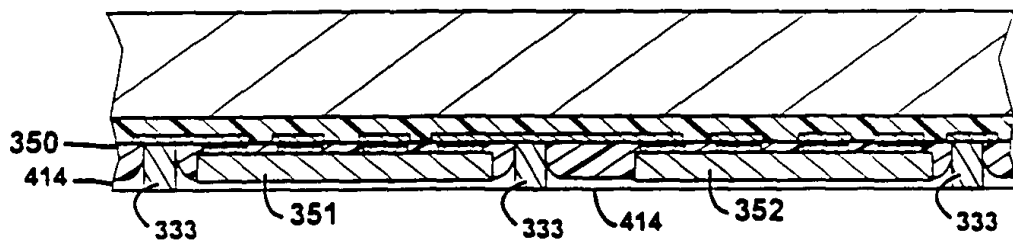


FIG.\_43

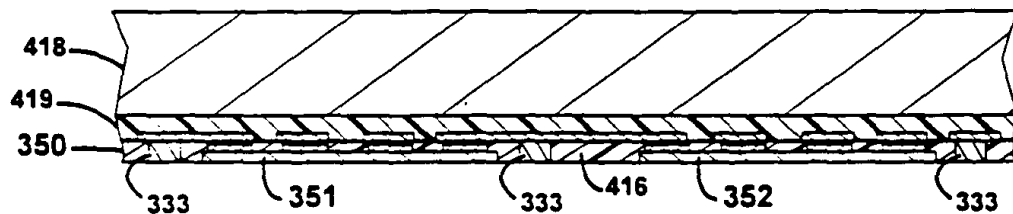


FIG.\_44

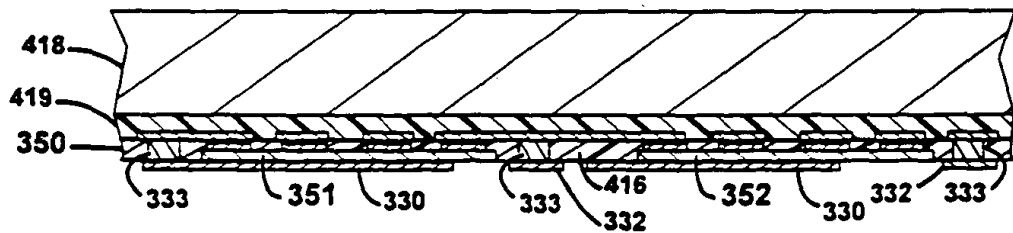
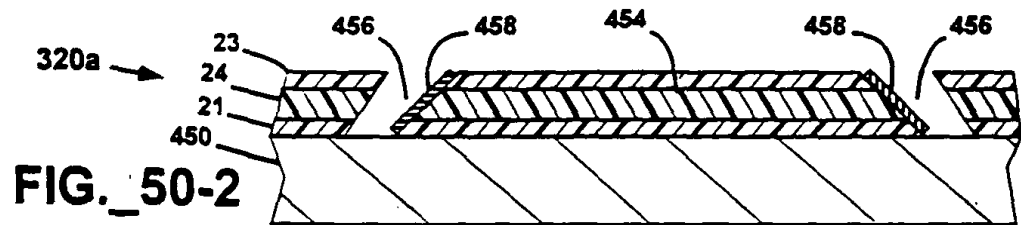
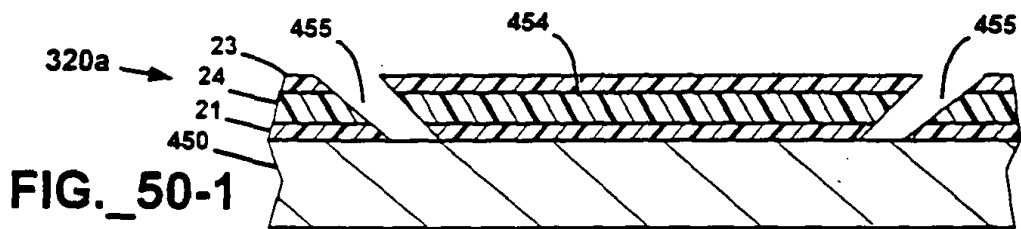
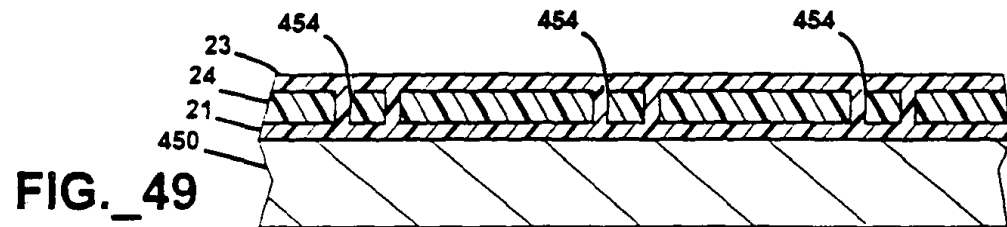
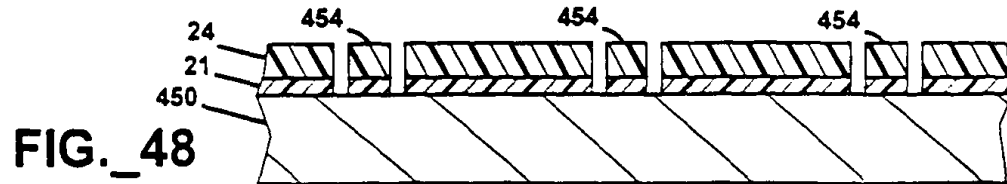
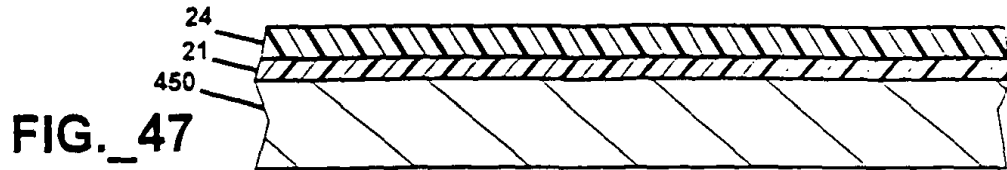
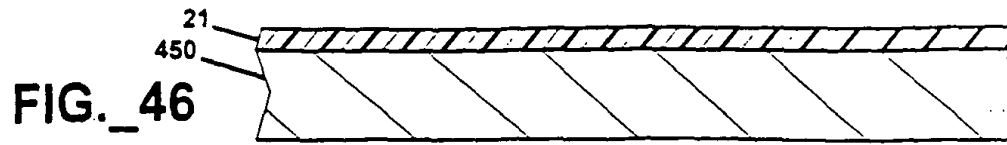
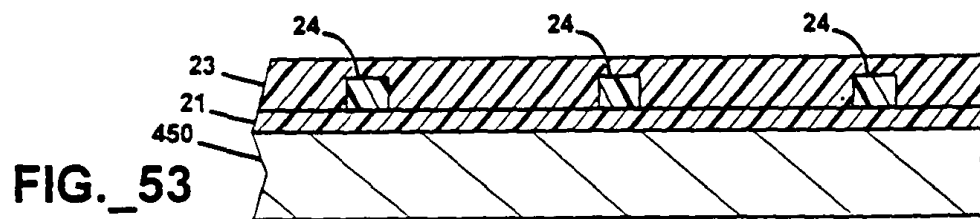
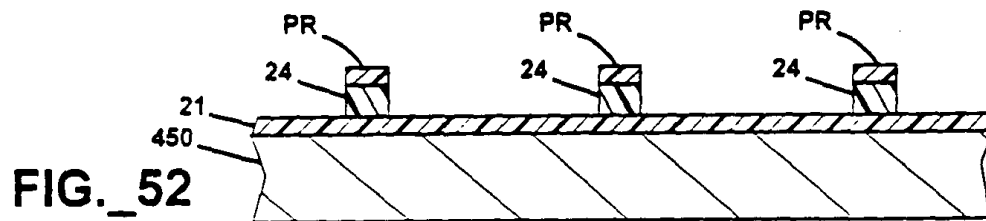
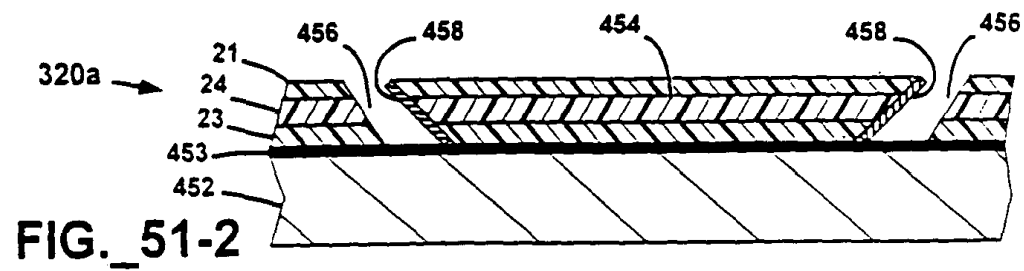
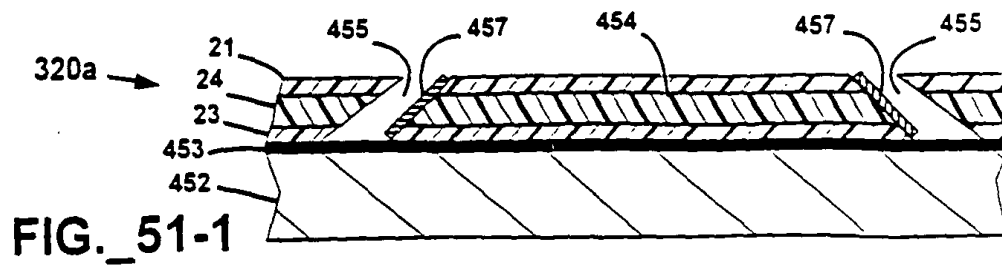


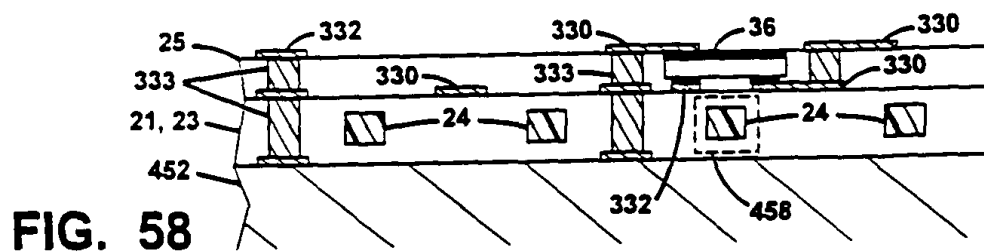
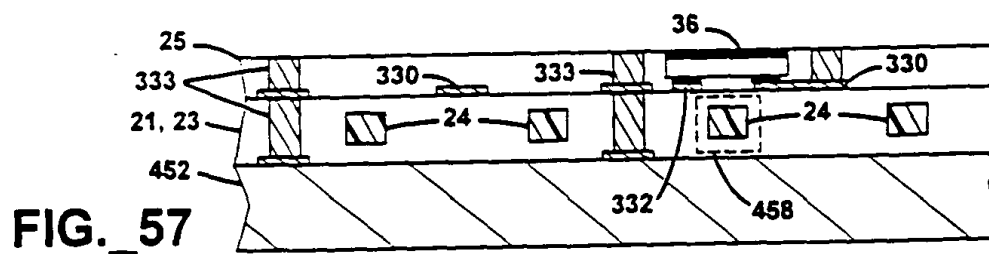
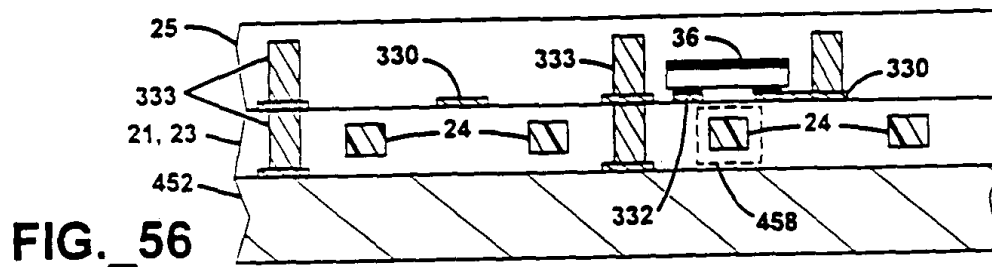
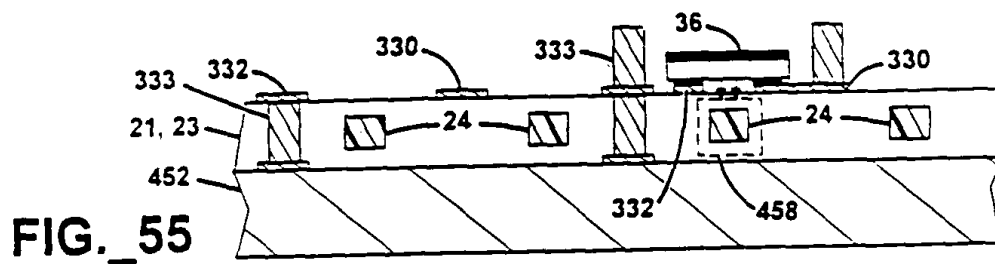
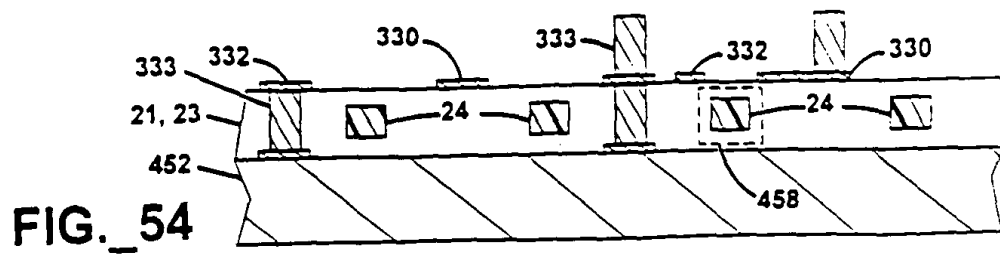
FIG.\_45

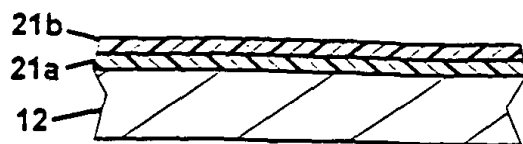
2019-09-29 09:49:49



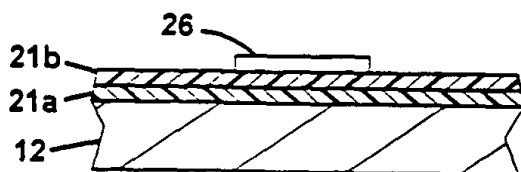




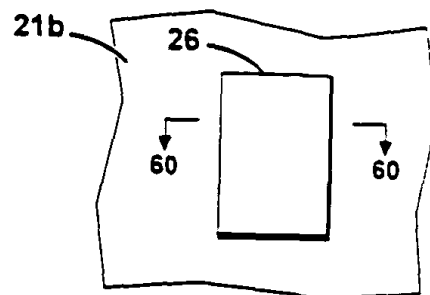




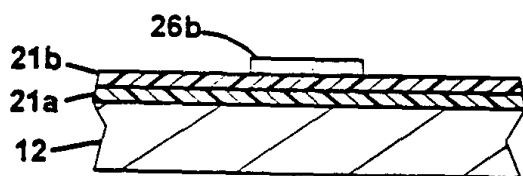
**FIG.\_59**



**FIG. 60**



**FIG. 61**



**FIG.\_62**

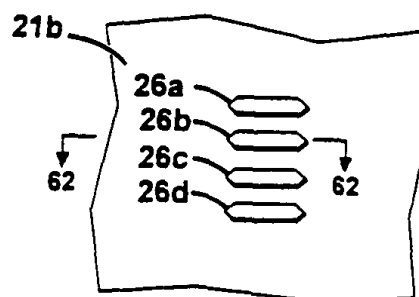
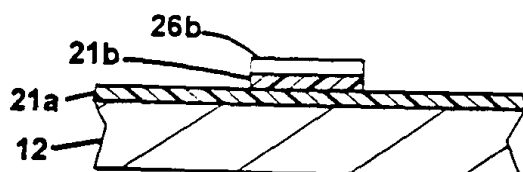
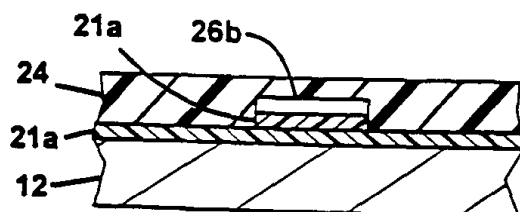


FIG. 63



**FIG. 64**



**FIG. 65**

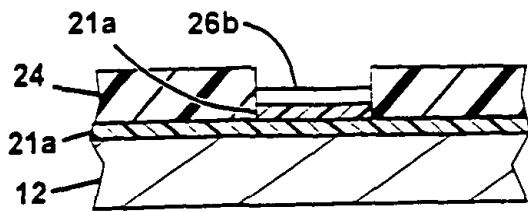


FIG.\_66

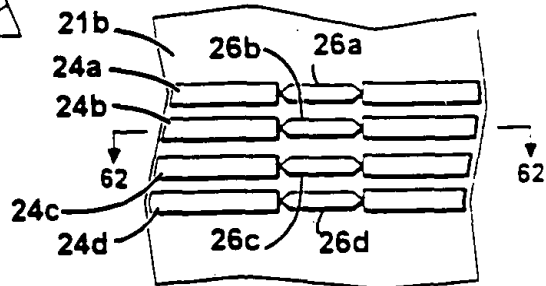


FIG.\_67

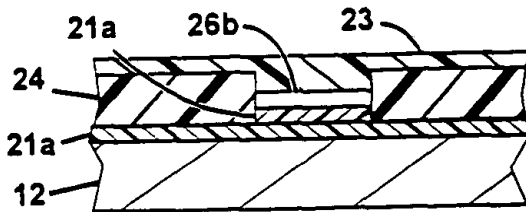


FIG.\_68

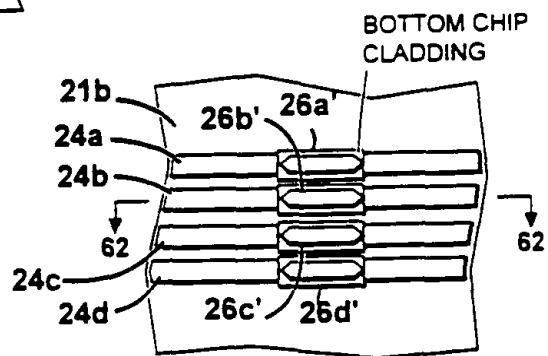
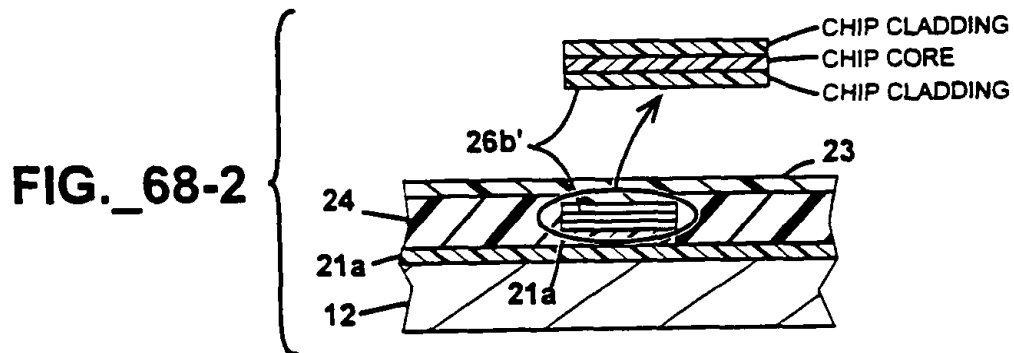


FIG.\_67-2



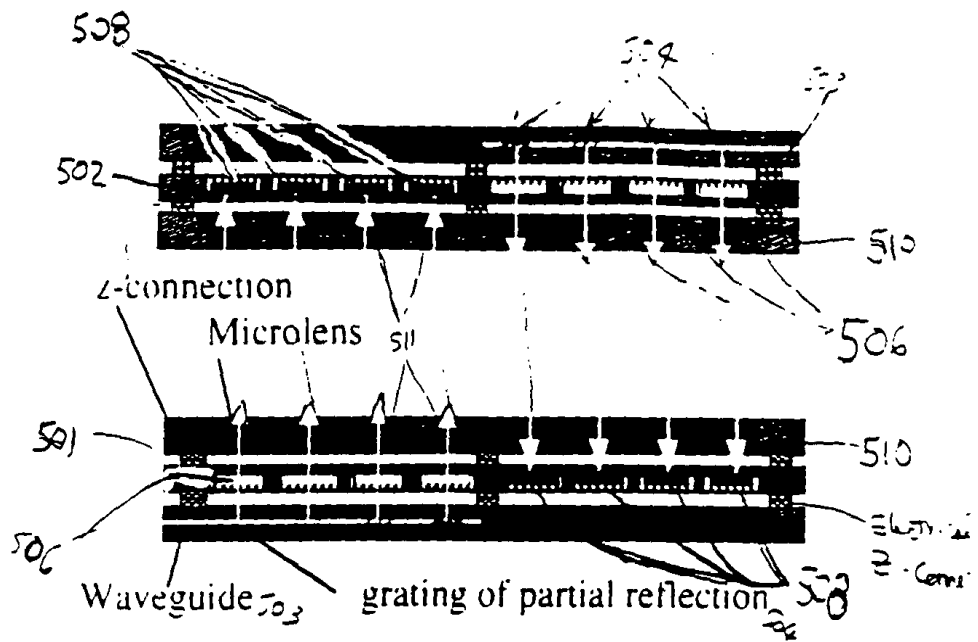


FIG. 69

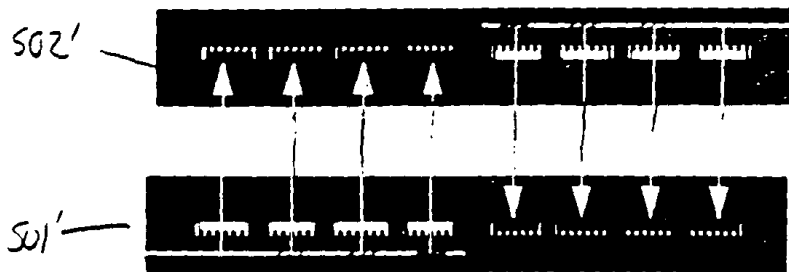
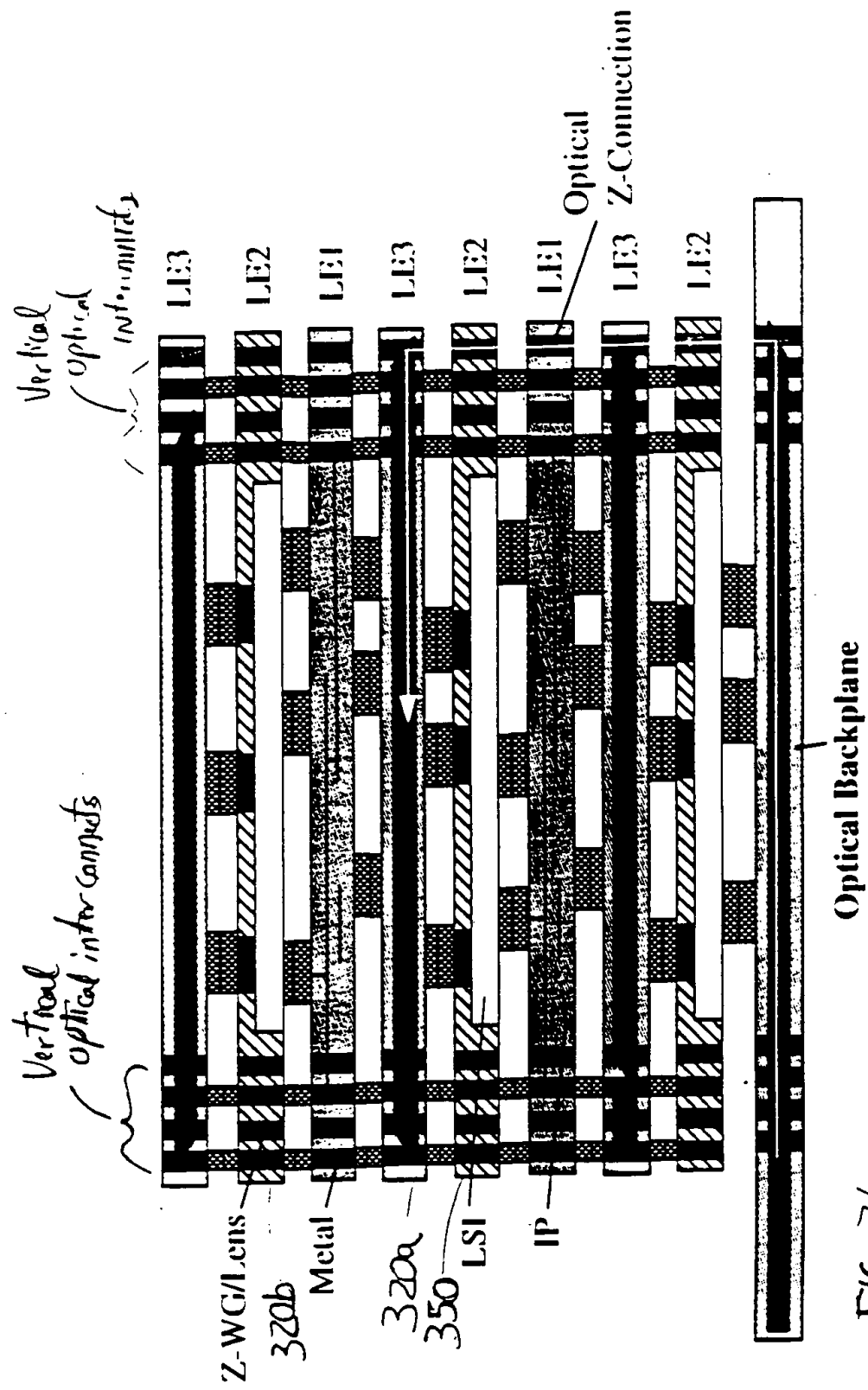


FIG. 70



11.9/11

with the following information: the name of the person to whom the information is being provided, the date and time of the information, and the name of the person providing the information.

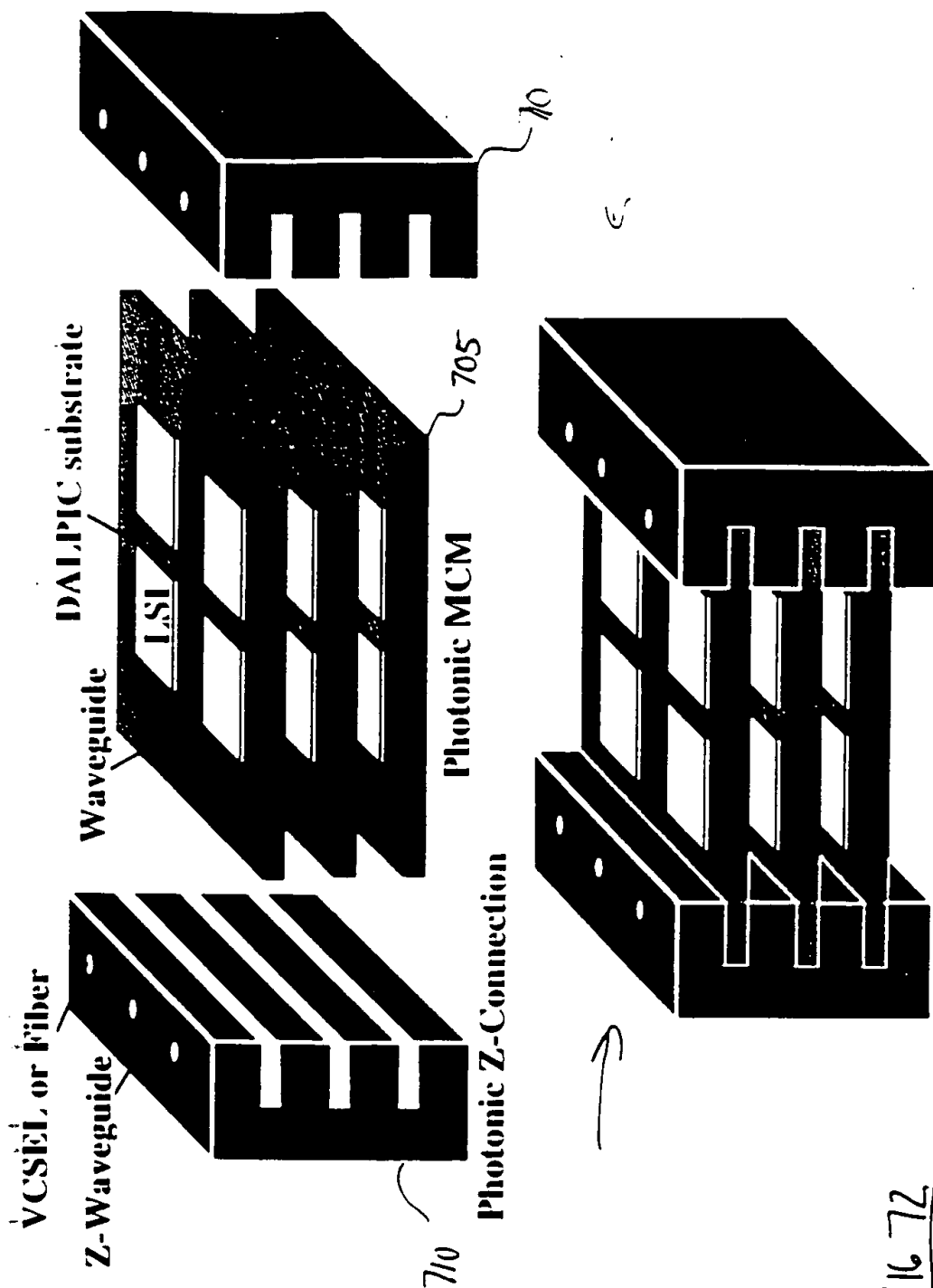
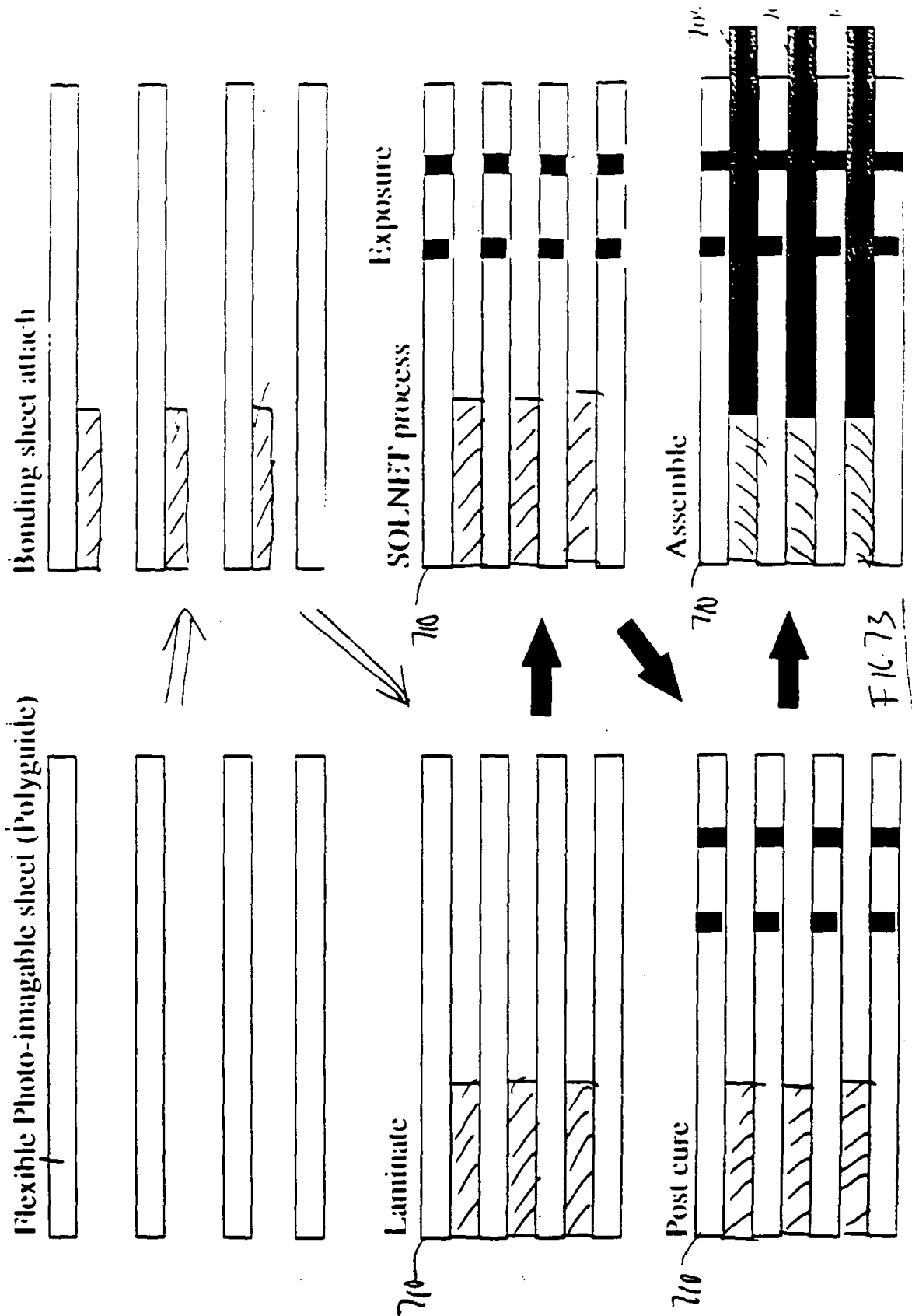
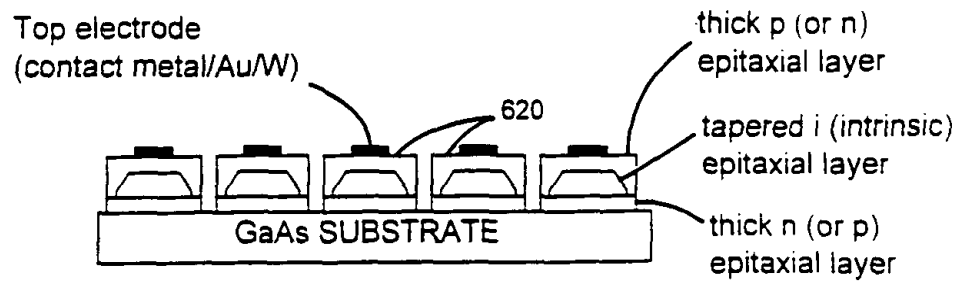
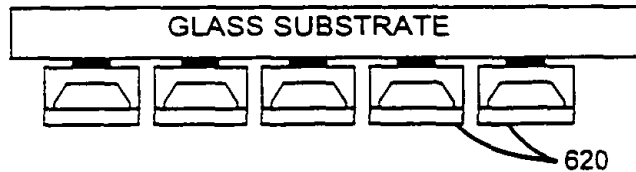


FIG 72

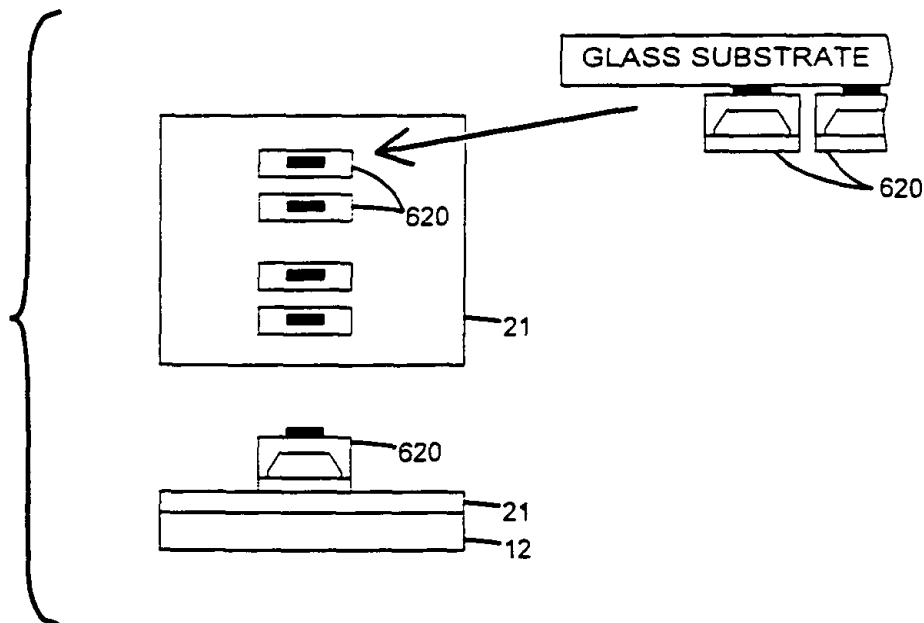




**FIG.\_74** (Epitaxial growth and patterning)



**FIG.\_75** (Epitaxial liftoff)



**FIG.\_76** (Transfer)



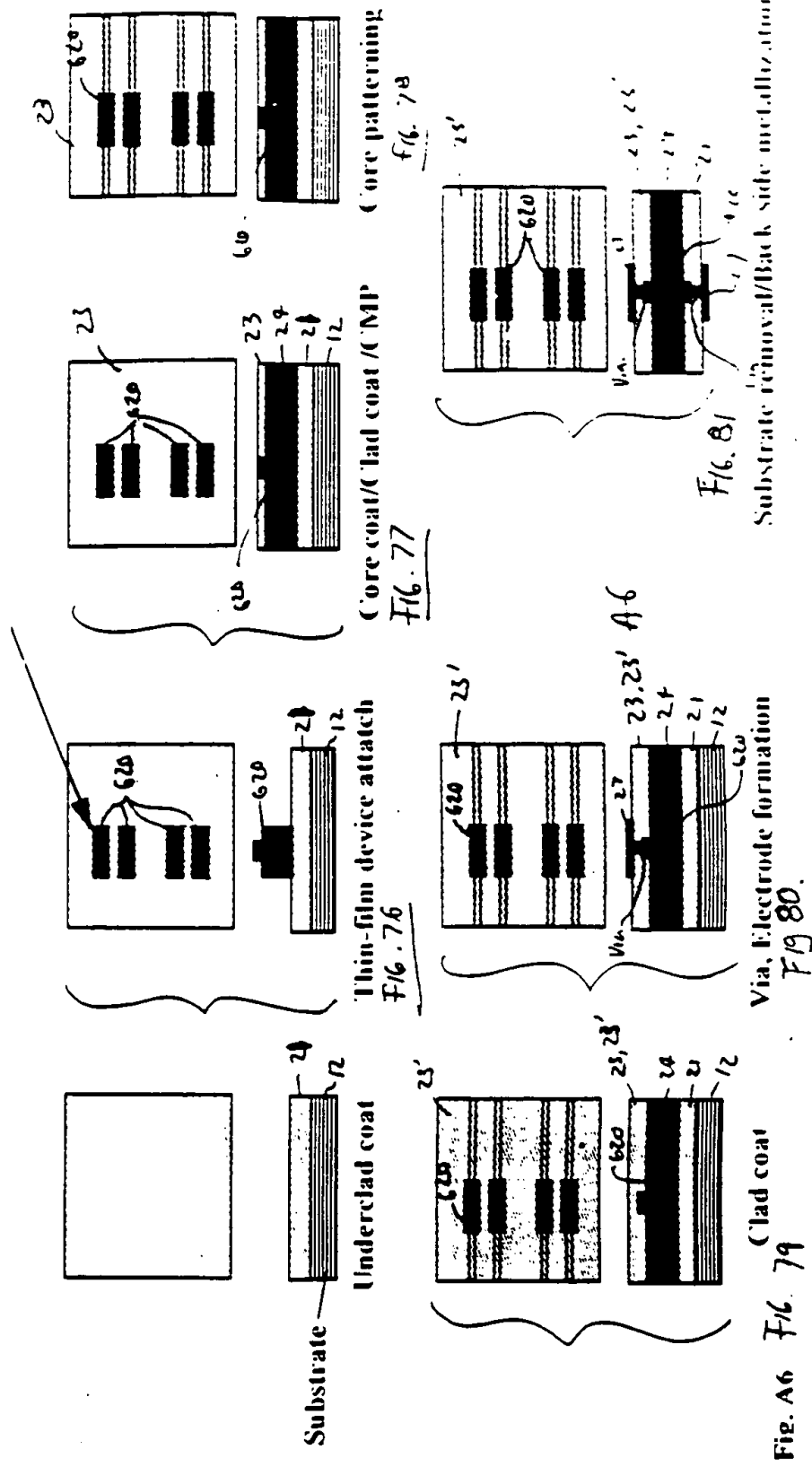


Fig. A6



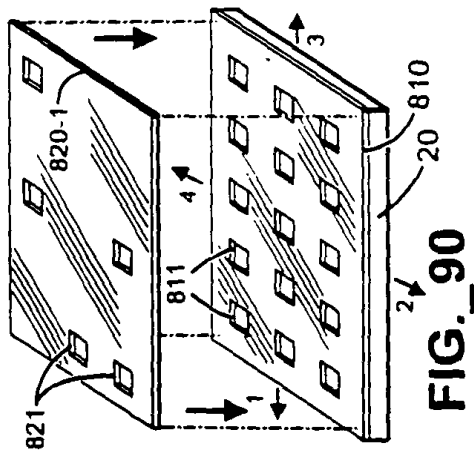


FIG. 90

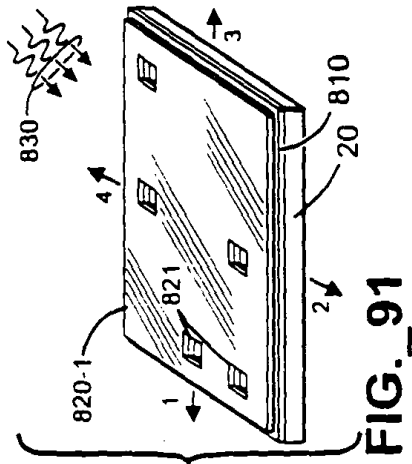


FIG. 91

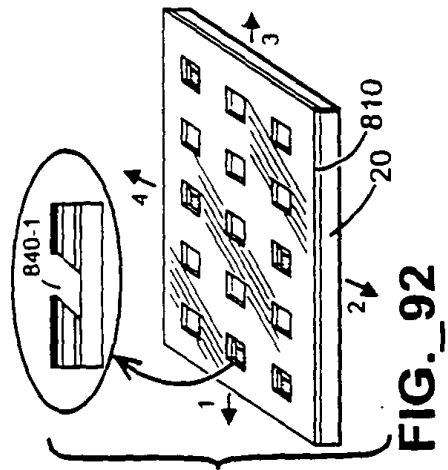


FIG. 92

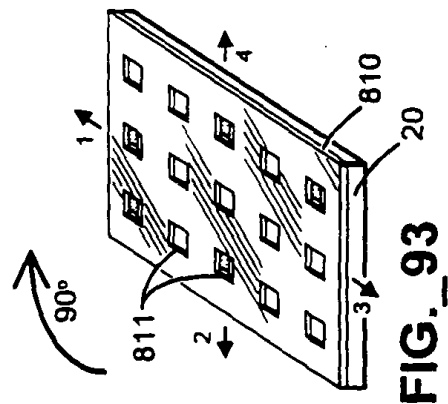


FIG. 93

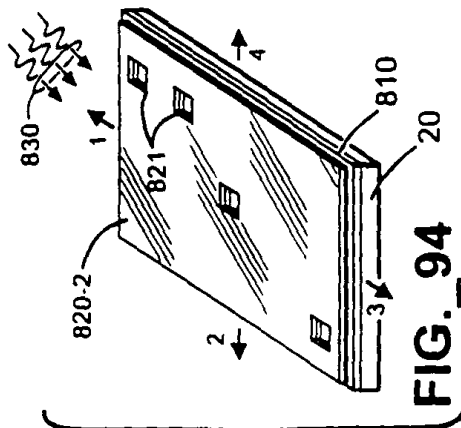


FIG. 94

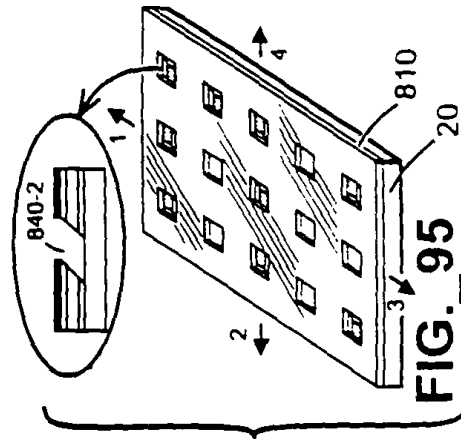
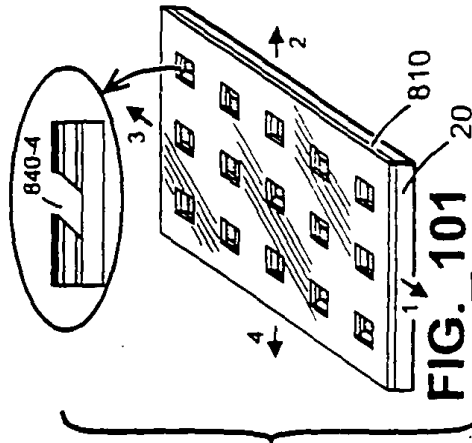
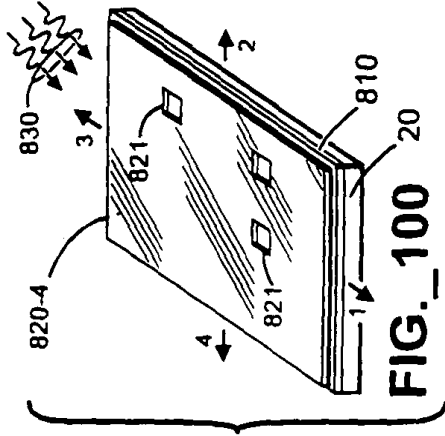
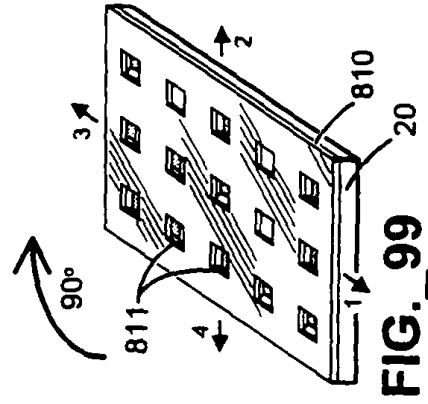
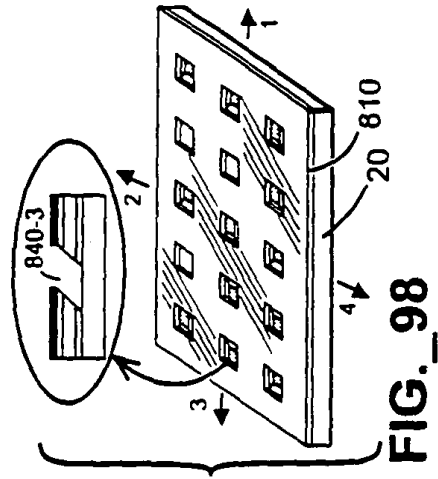
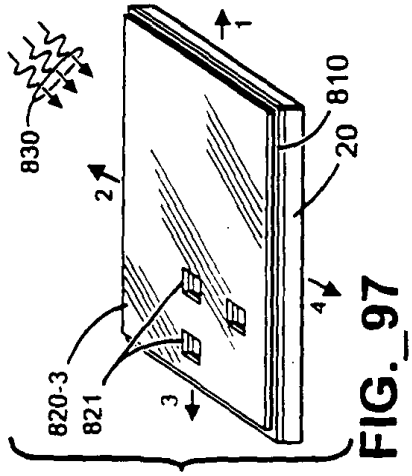
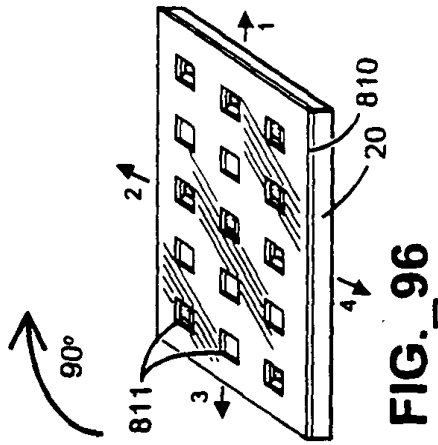
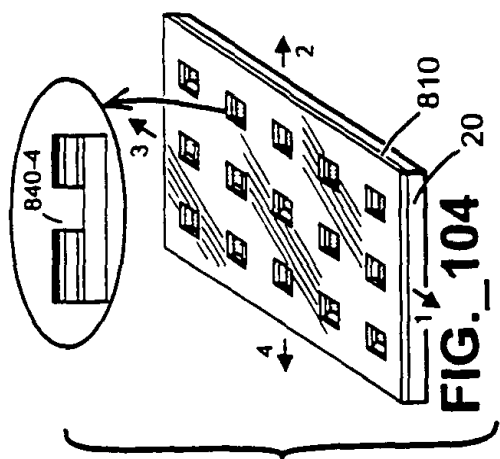
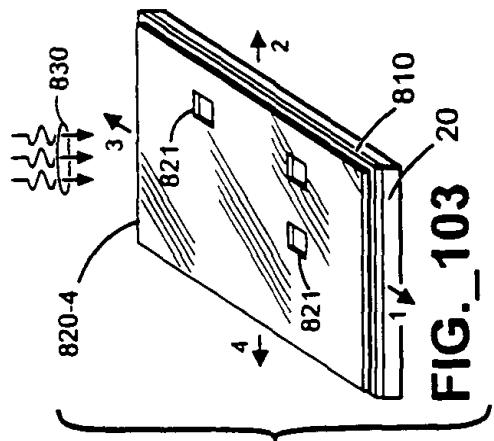
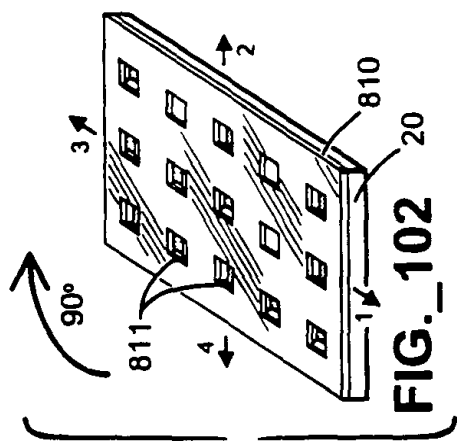


FIG. 95





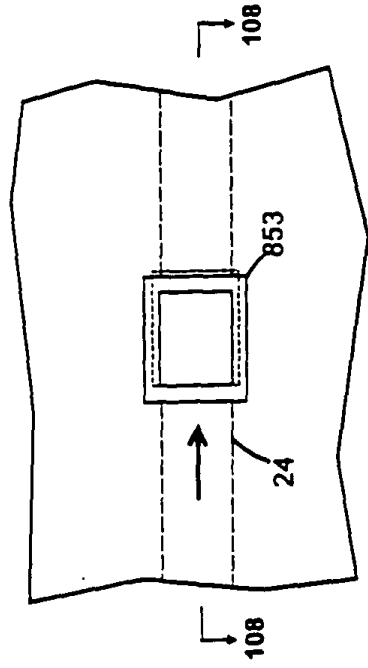
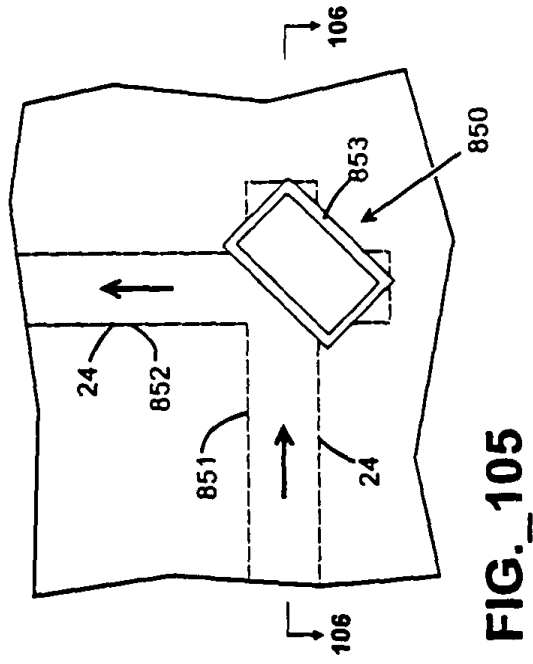


FIG. 107

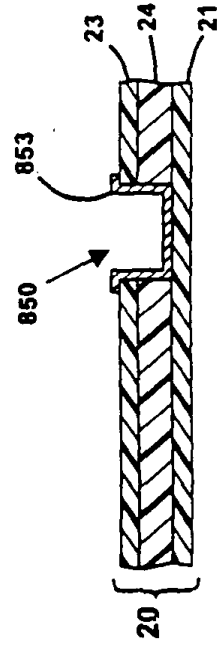


FIG. 106

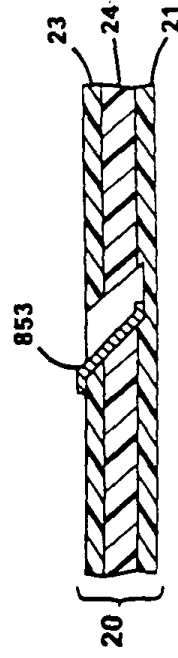


FIG. 108

## GS CX/CXX OE Solution --- OE-3D-Stack

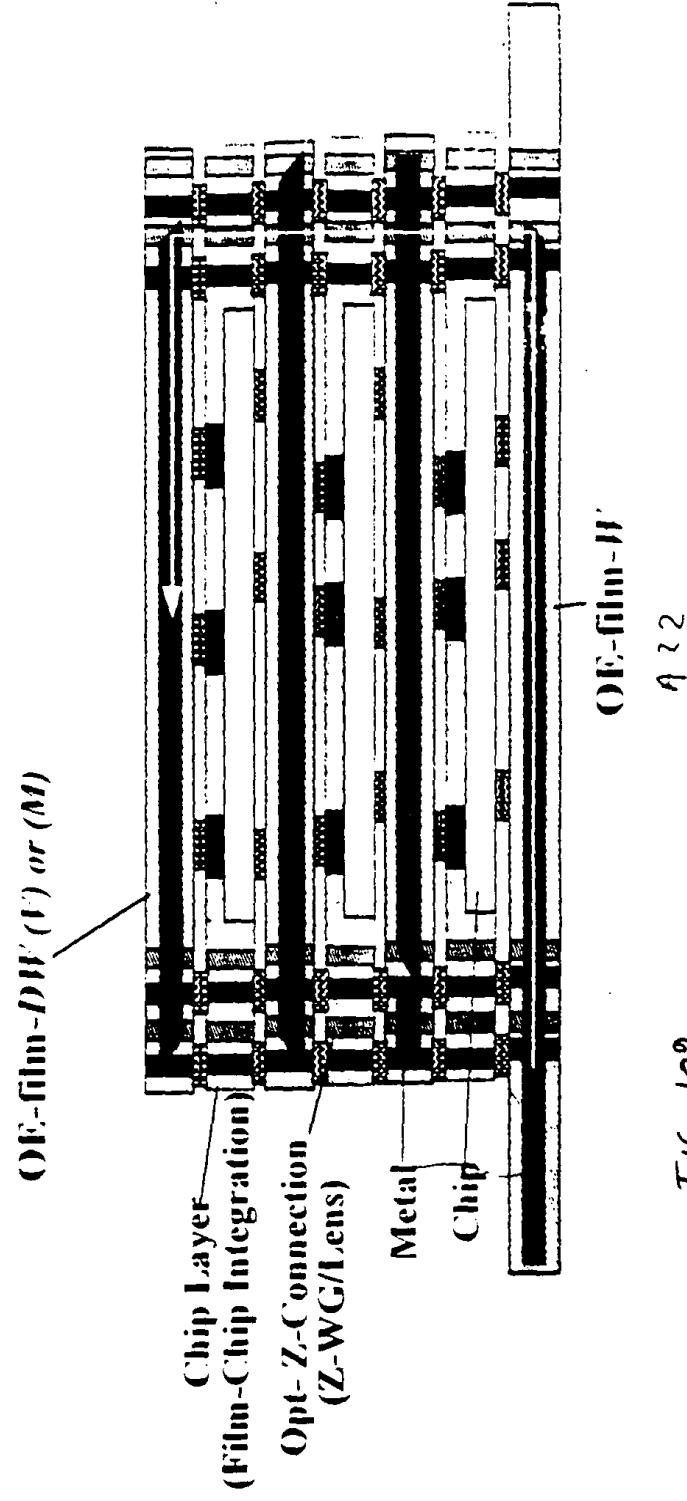


FIG. 109

204049-236263

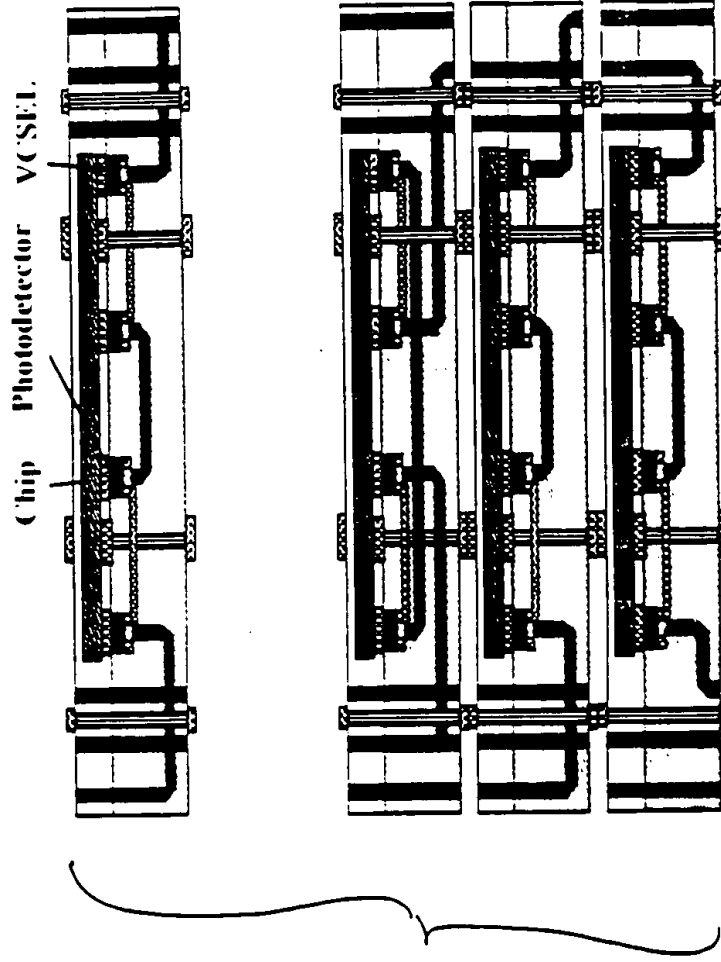


Fig. 110

A23

(2/23/99) AA1 Detail picture Example for 3D-stack'

(New version of the AA1 of 2/5/99)

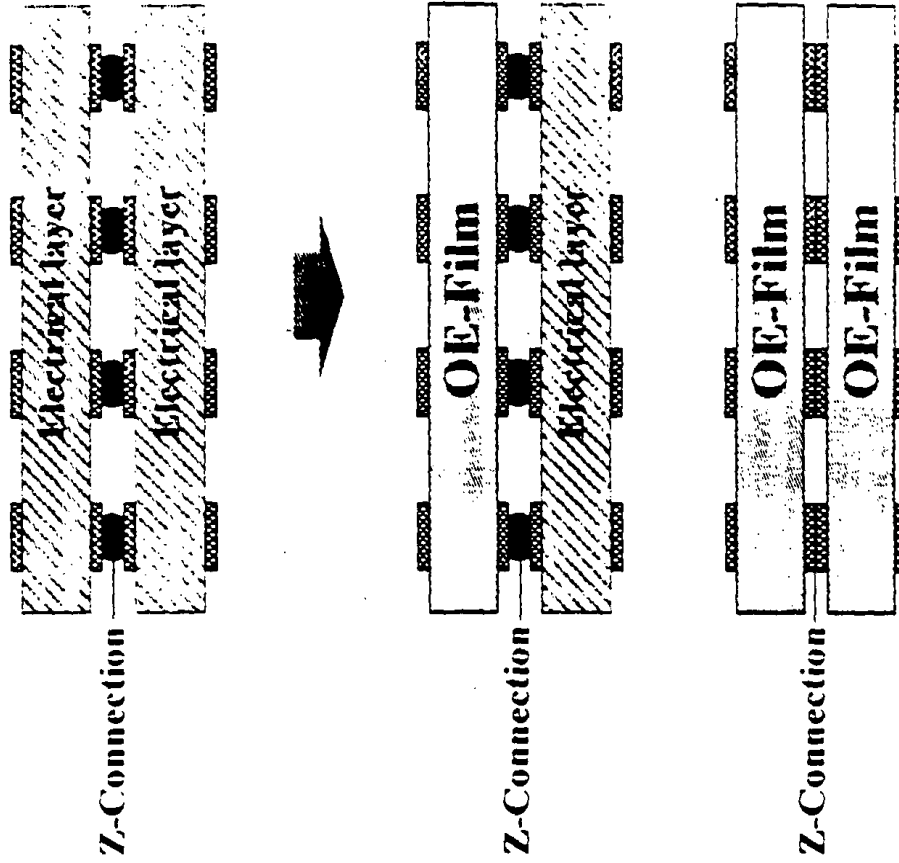


A24

**(2/23/99) AA2 Detail picture Example for 3D-stack'**

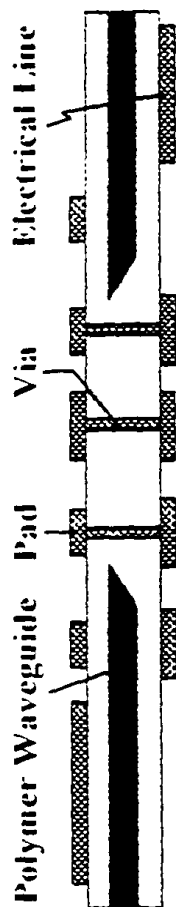
**(New version of the AA2 of 2/5/99)**

FUJITSU Computer Packaging Technologies, Inc. **Film/Z-Connection Application to OE-Substrate**



2/23/99-added 1

OE-Films



OE-film-W

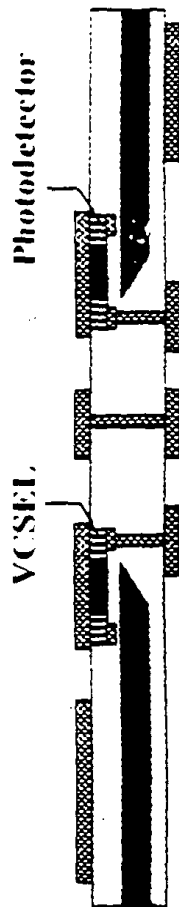
Fig. 113



OE-film-D

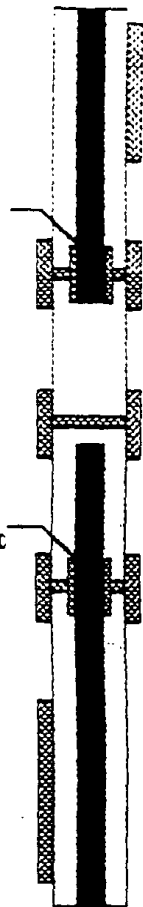
Fig. 114

A8



OE-film-DW(V)

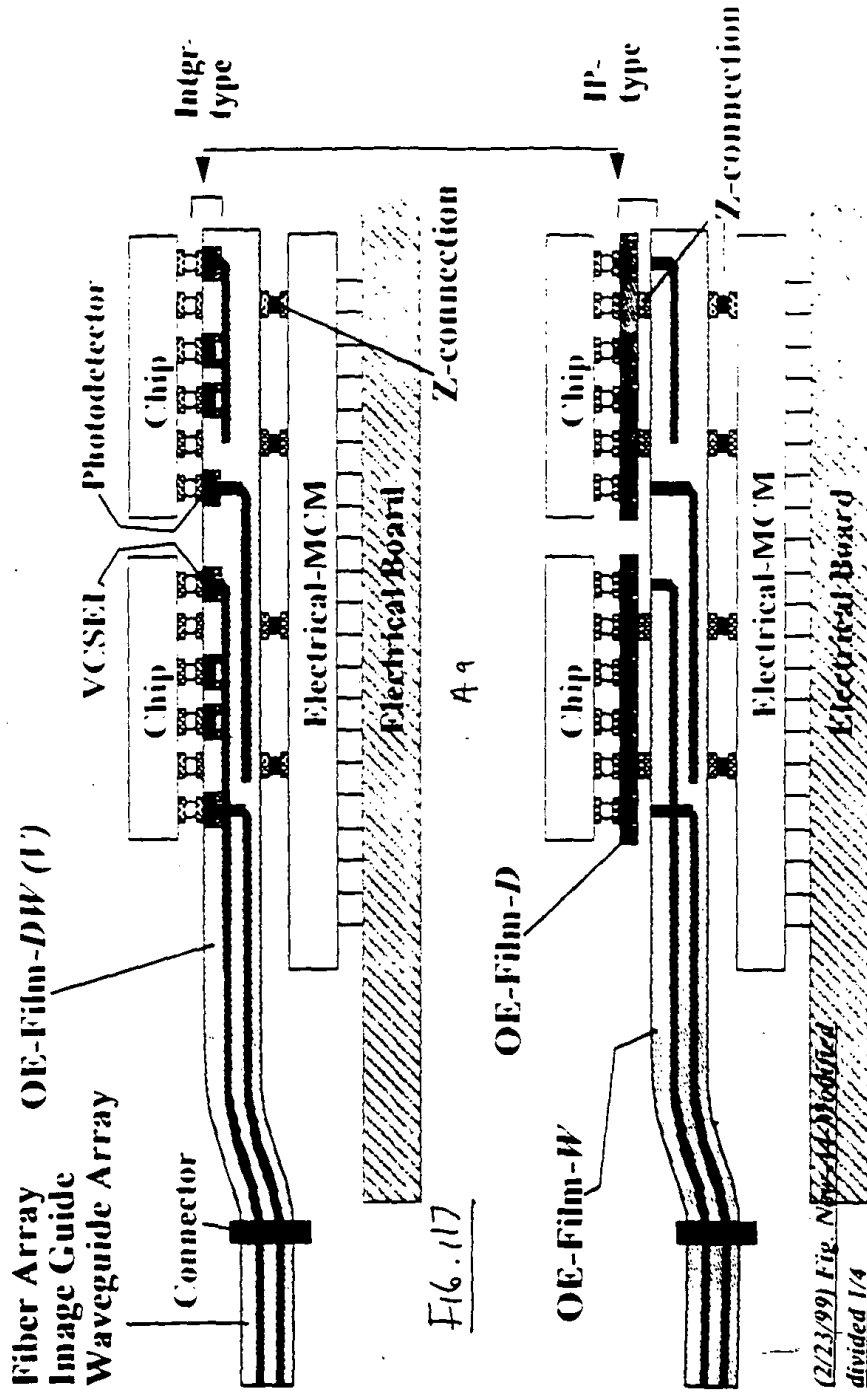
Fig. 115



OE-film-DW(M)

2/17/99-added 2

Fig. 116



(2/23/99) Fig. New-44 Modified divided 1/4

**FOLM**

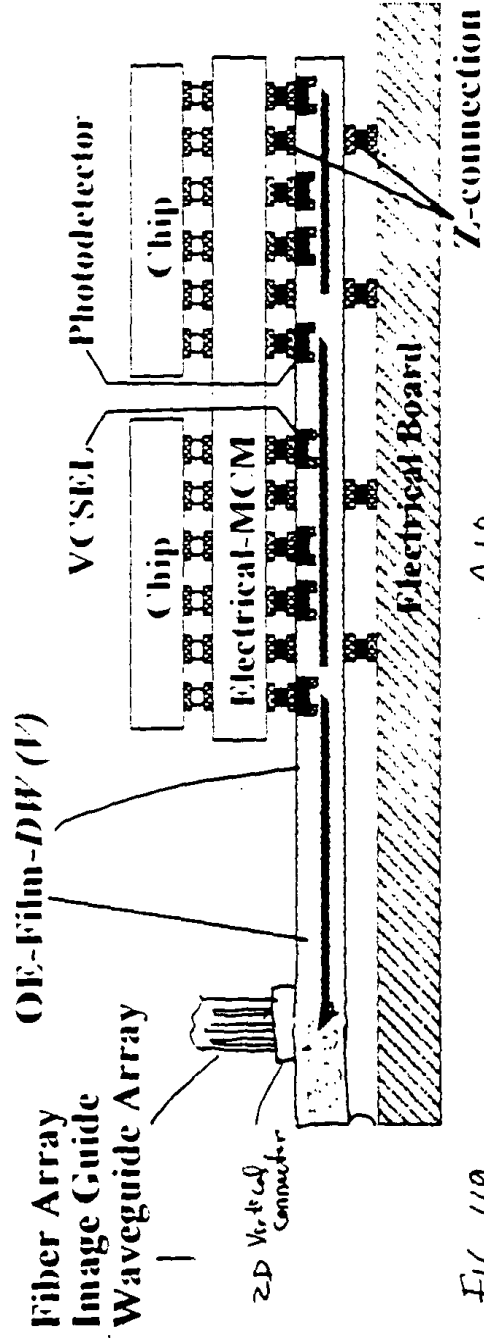


Fig. 119

A 10

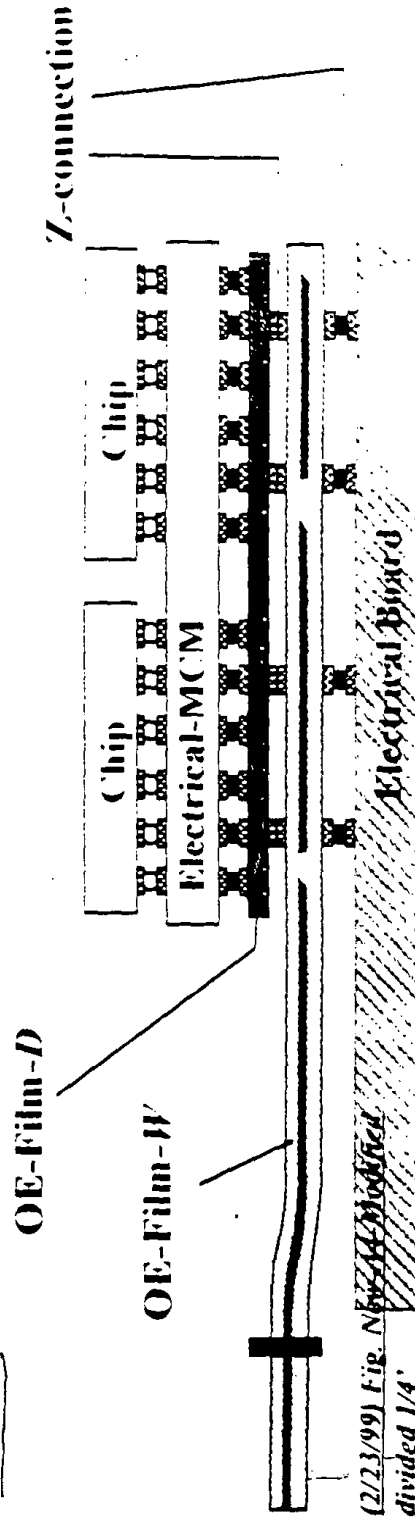
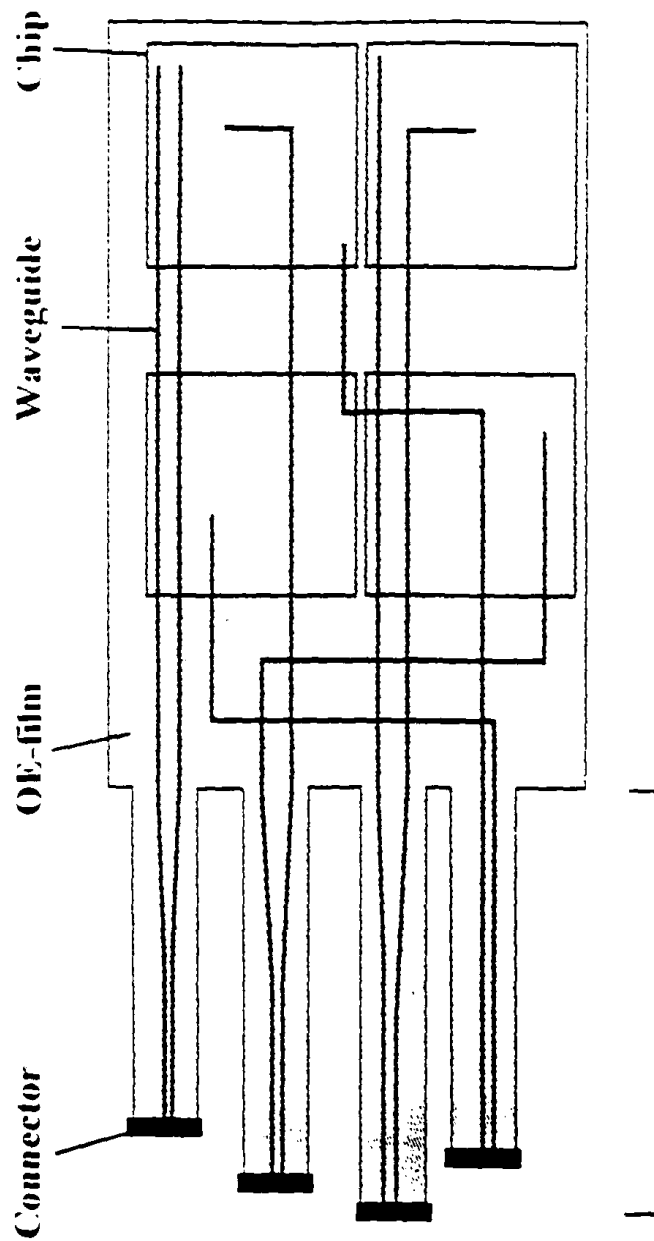


Fig. 120

# **FOLM with Optical Path Length Controller, Connector Buffer**



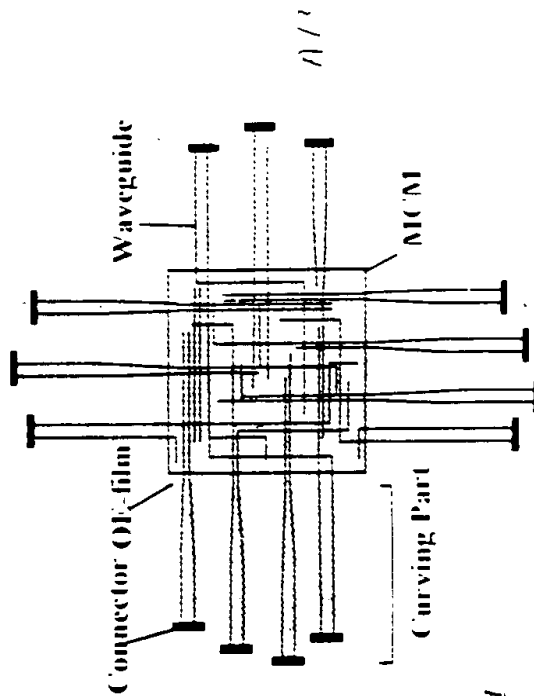
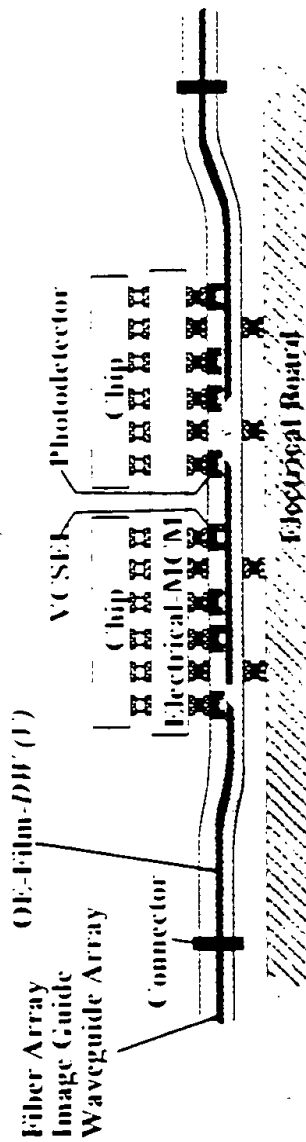
A 11

Curving Part

FIG. 121

(2/17/99) Fig. New-A4-Modified  
divided 2/4

FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**FOILM with Optical Path Length Controller, Connector Buffer**



(2/23/99) Fig. New-A4-Modified  
 divided 2/4'

FUJITSU Computer Packaging Technologies, Inc. — FCPT  
**FOLM with 2D Waveguide Connector**

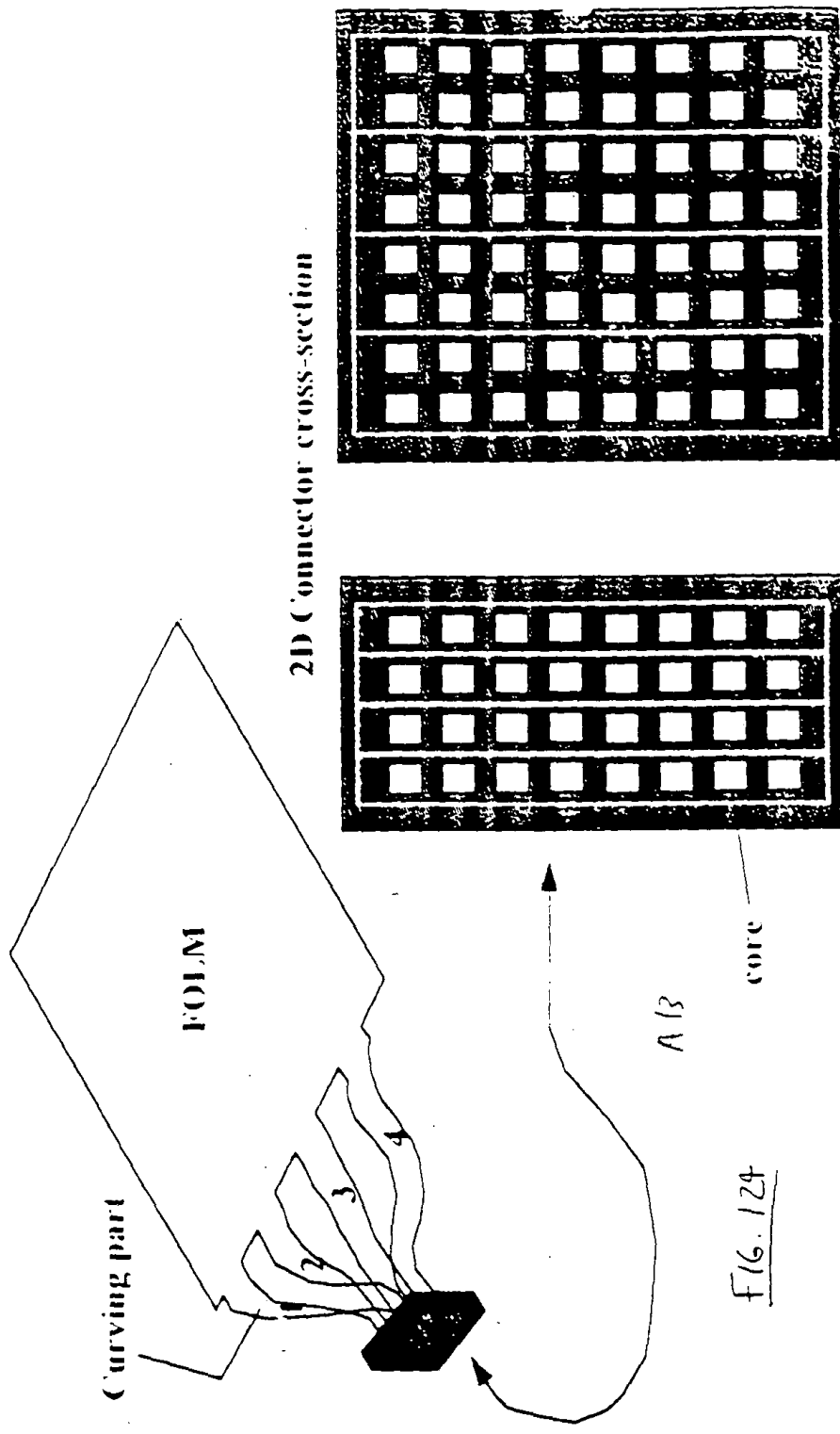


FIG. 124

(223/99) Fig. New-A4-Modified  
 divided 3/4

(for Single-layer waveguide) (for 2 layer waveguide)



204040-28529250

FUJITSU Computer Packaging Technologies, Inc. — FCPT

## FOLM: High-Speed Option

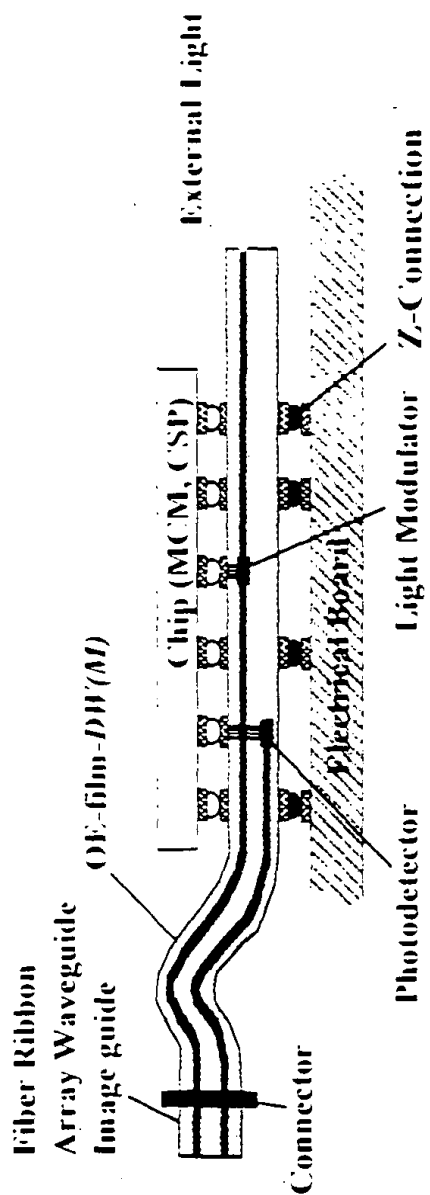
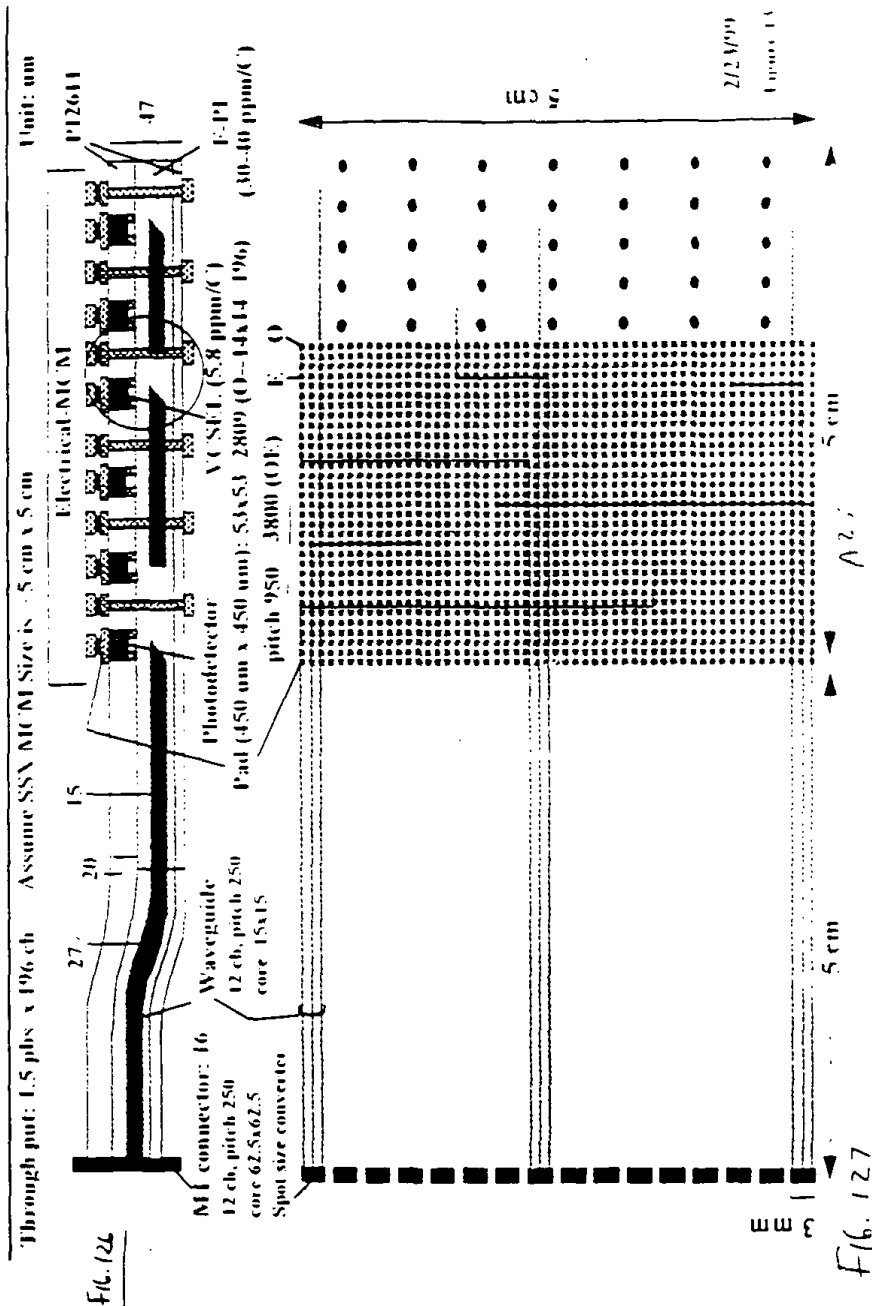


Fig. 125

A14

(2/17/99) Fig. New-A4-Modified  
divided 4/4

## FOLM Structure Example (Overall)



FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**FOLM Structure Example (VCSEL part)**

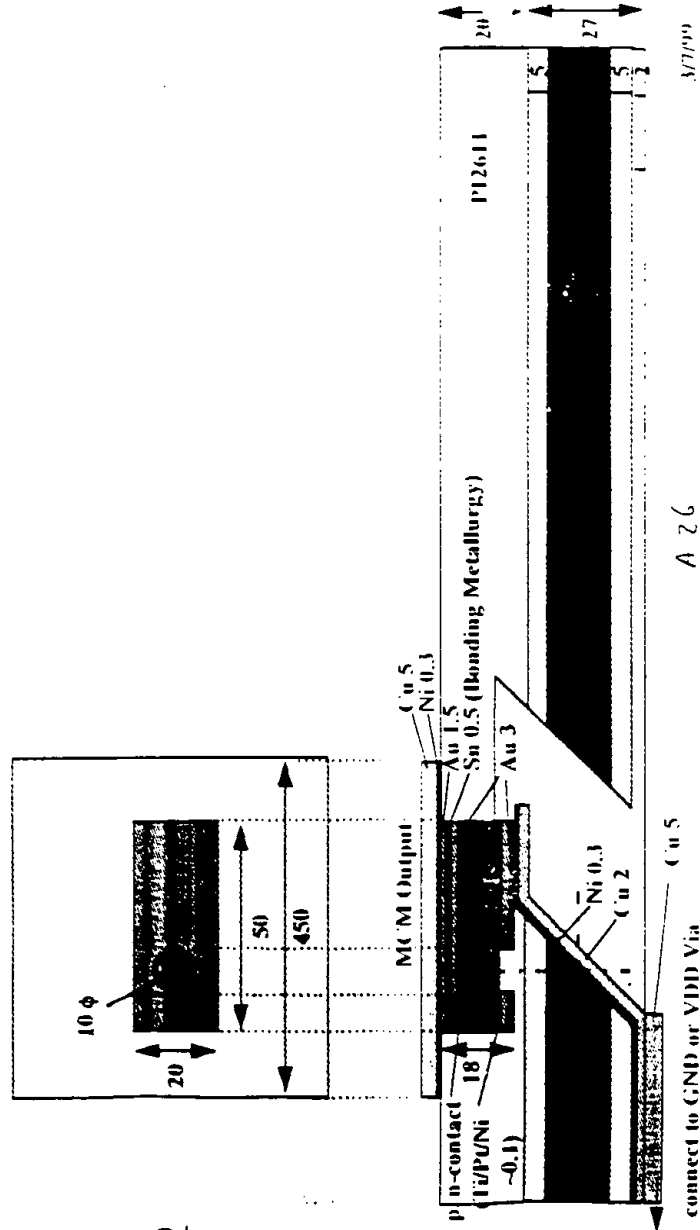
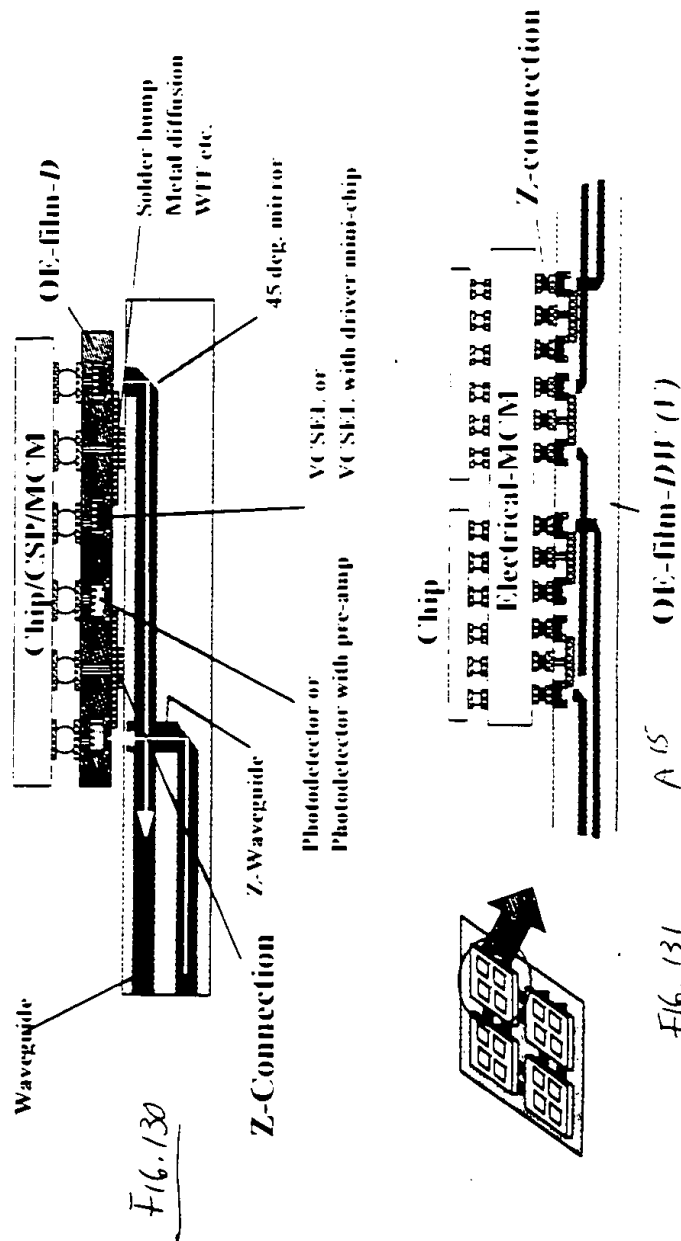


Fig. 129

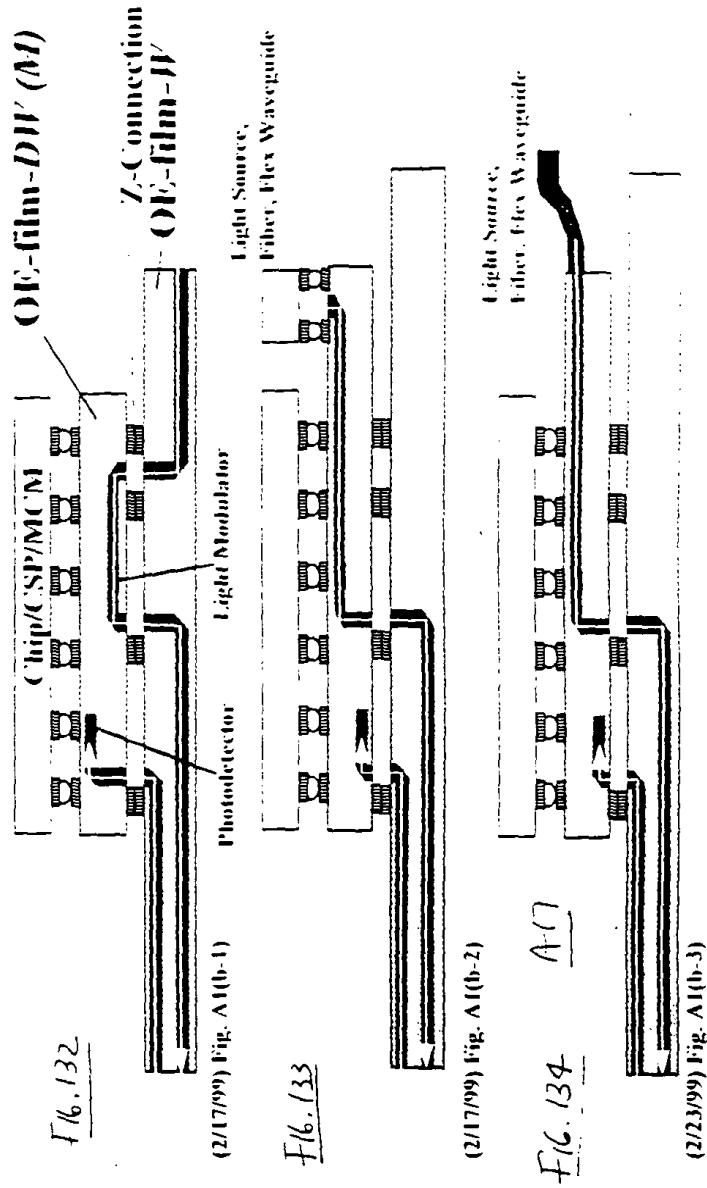
Unit : μm

# OE-film: OE-IP, OE-Film-MCM



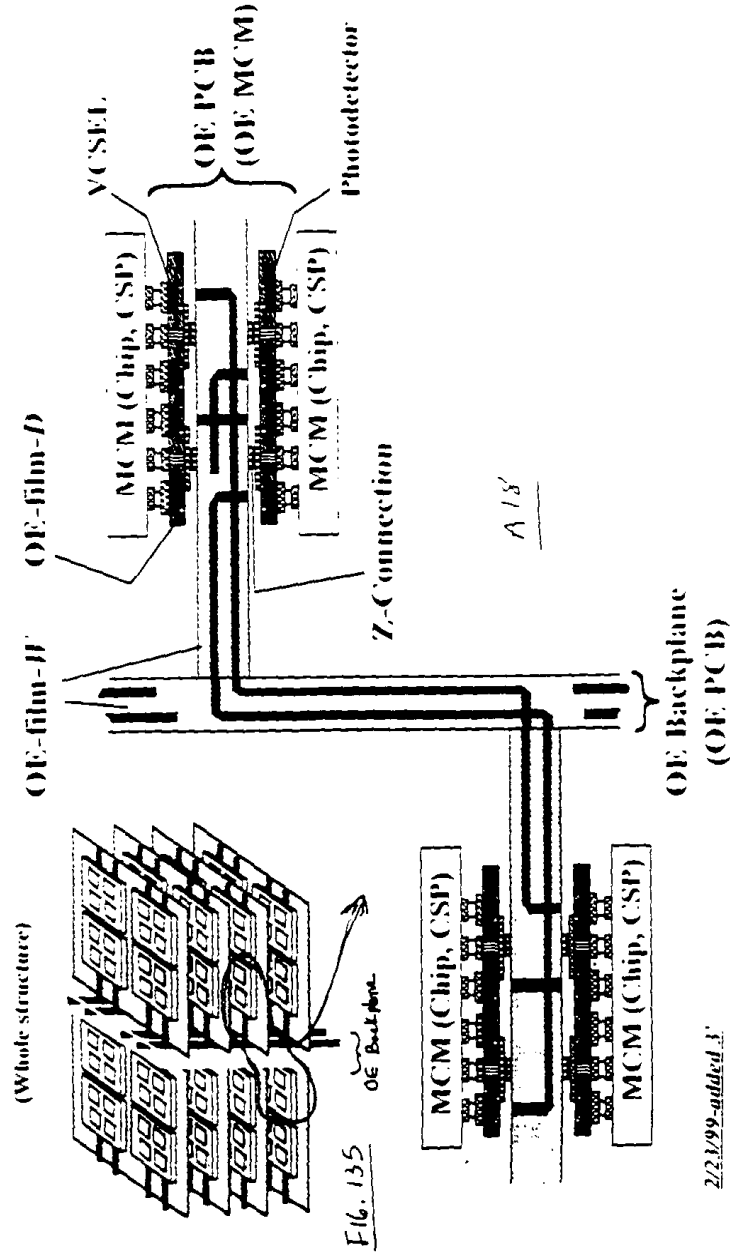
(2/23/99) Fig. New-AI-Modified

<sup>62</sup>  
Fujitsu Computer Packaging Technologies, Inc. — FCPT  
OE-film: Light Modulator Transmitters



Examples of Light Modulators: Electro-Optic (E.O.) Modulator, Electro-Absorption (E.A.) Modulator

FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**OE-film: Both-Side Packaging**



## Direct Jump from LSI

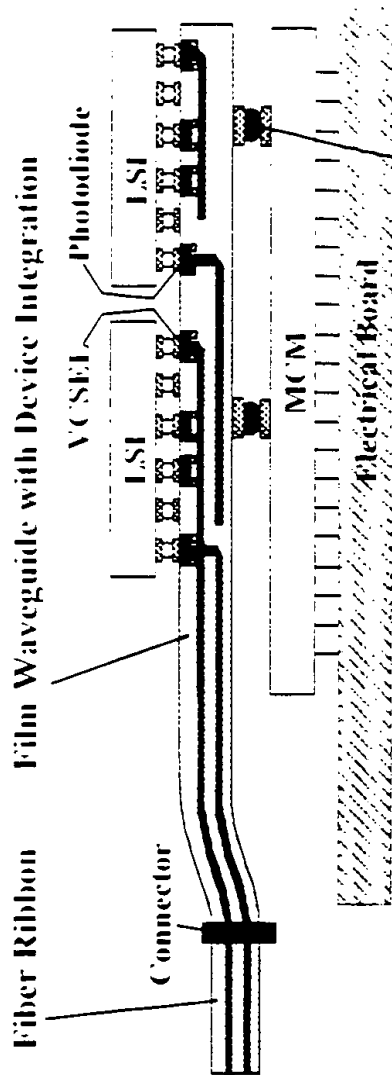
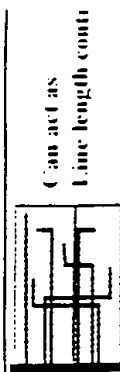


Fig. 136

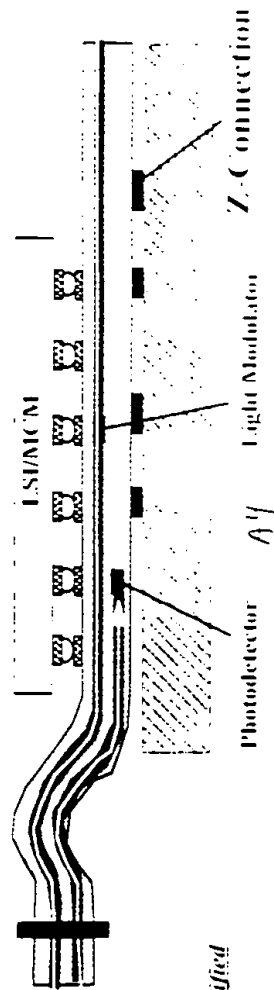
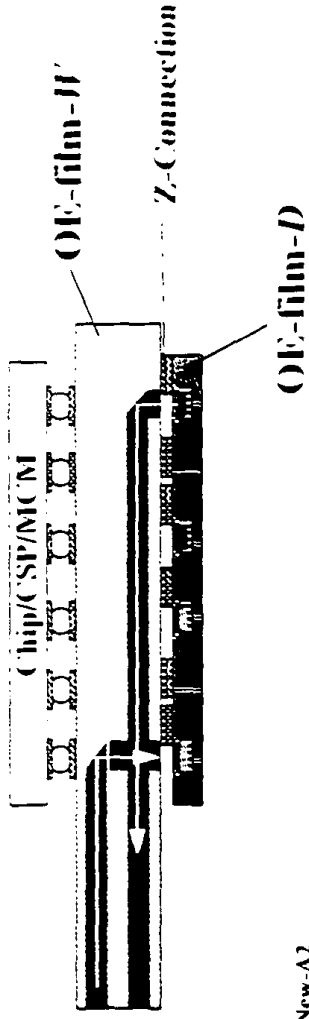


Fig. 137

Fig. New-14-Modified

Computer Packaging Technologies, Inc. FCPT

# OE-IP is Placed on the Opposit Side



(2/23/99) Fig. New-A2 Fl6.138



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FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**OE MCM**

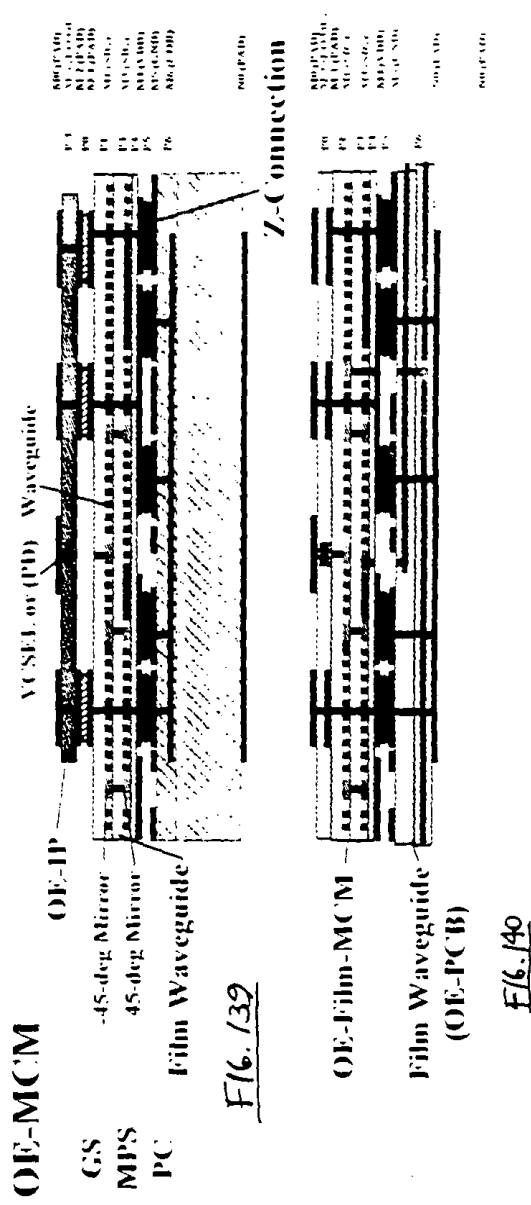


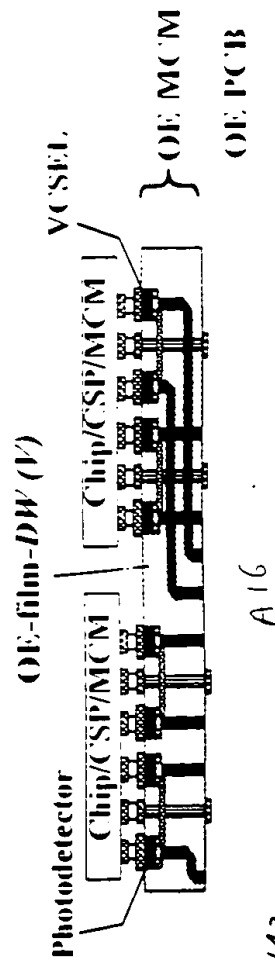
Fig. A5-Modified

AS

## OK-film: Smart Pixel



Fig. 141



File 142

FCP  
**OE-Film/OE-Film Stack --- Back-Side Connection**

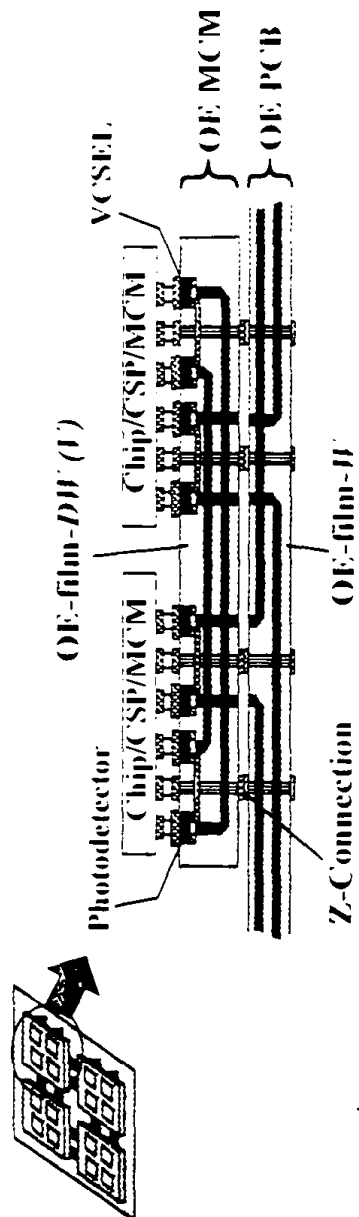
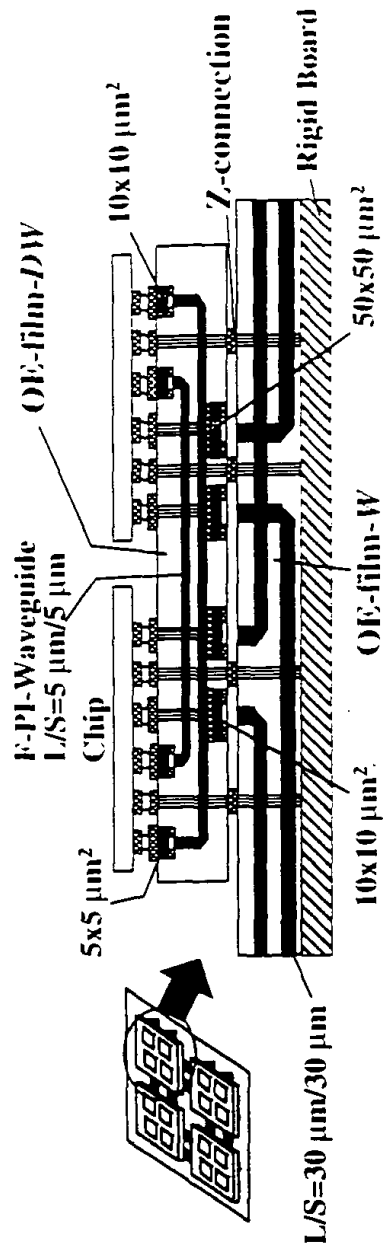


FIG. 143

# FCPT

## OE-Film/OE-Film Stack --- Back-Side Connection



DI

Fig. 144

FUJITSU Computer Packaging Technologies, Inc. — FCPT  
**OE-MCM/OE-Bord Stack**

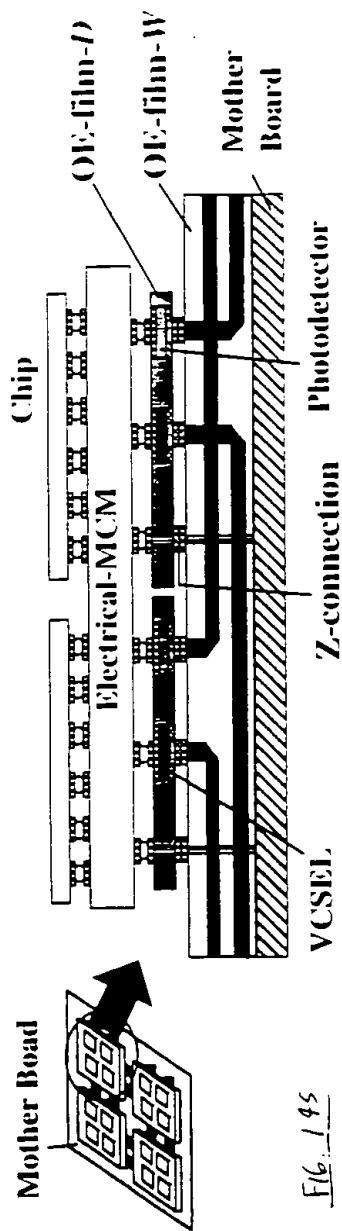


Fig. 145

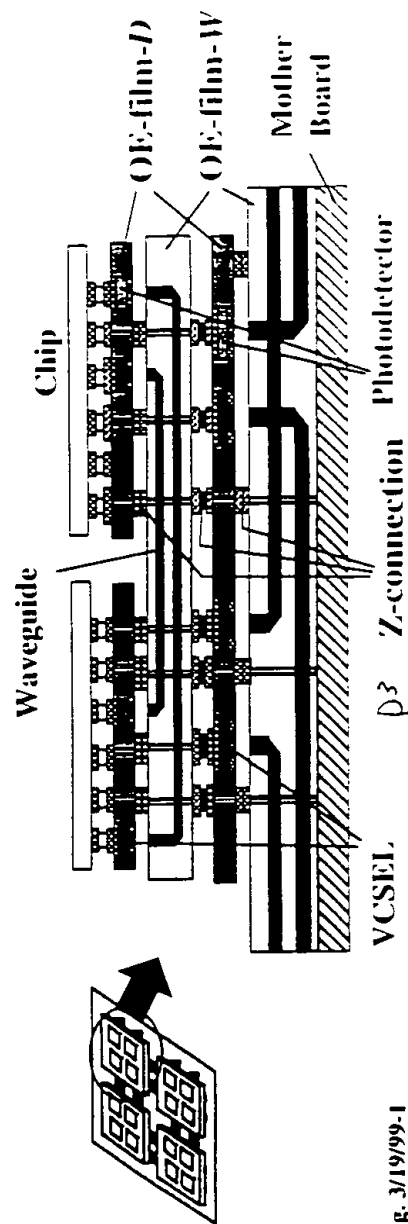
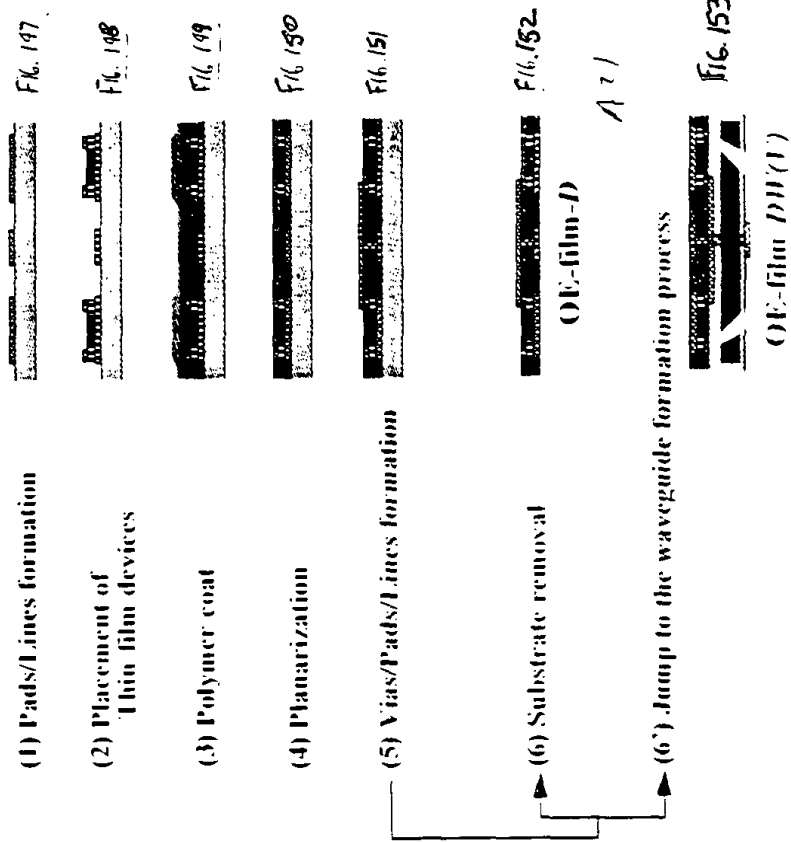


Fig. 3/19/99-1

# Device Integration Process



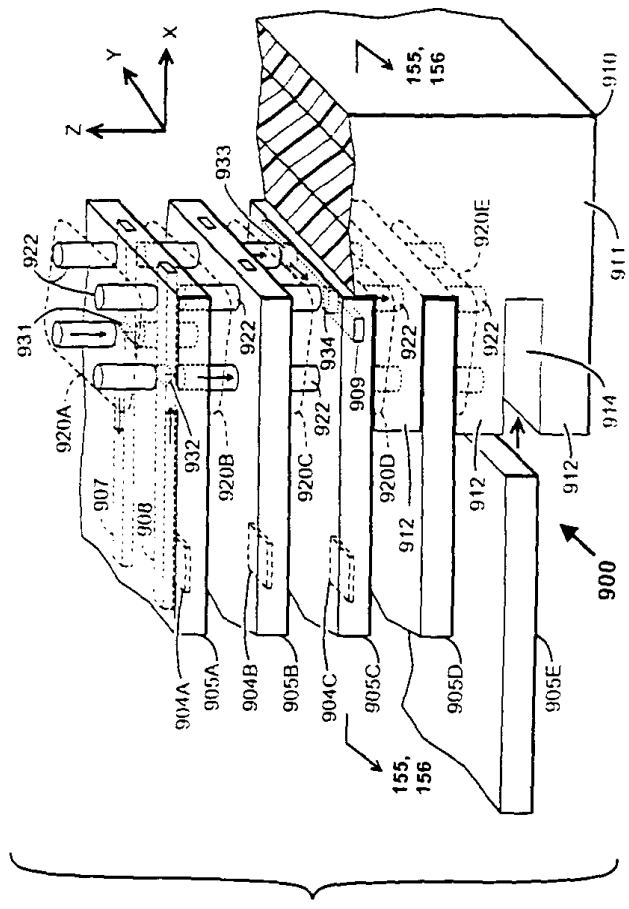


FIG. 154

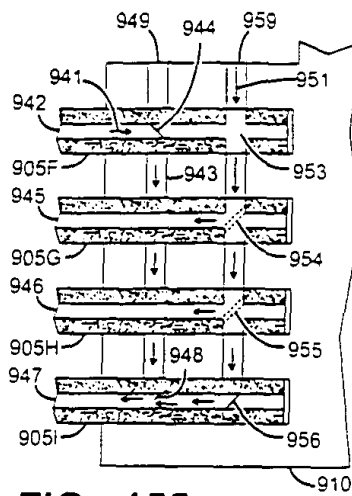


FIG. 155

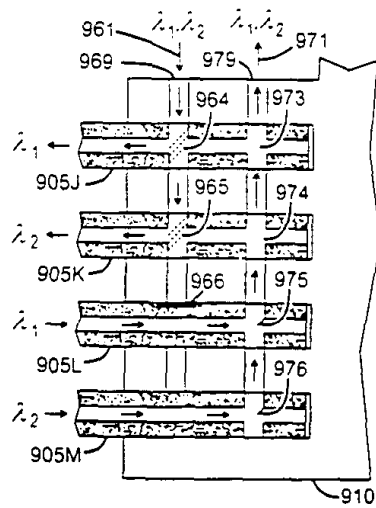


FIG. 156-1

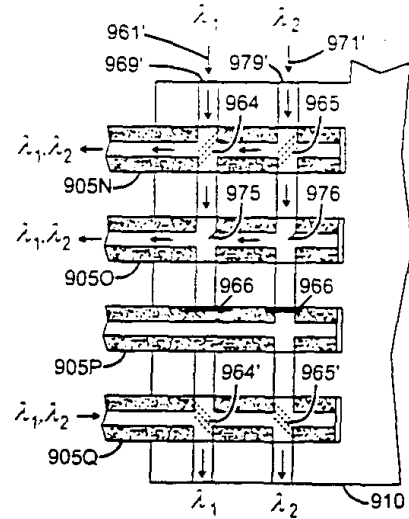


FIG. 156-2



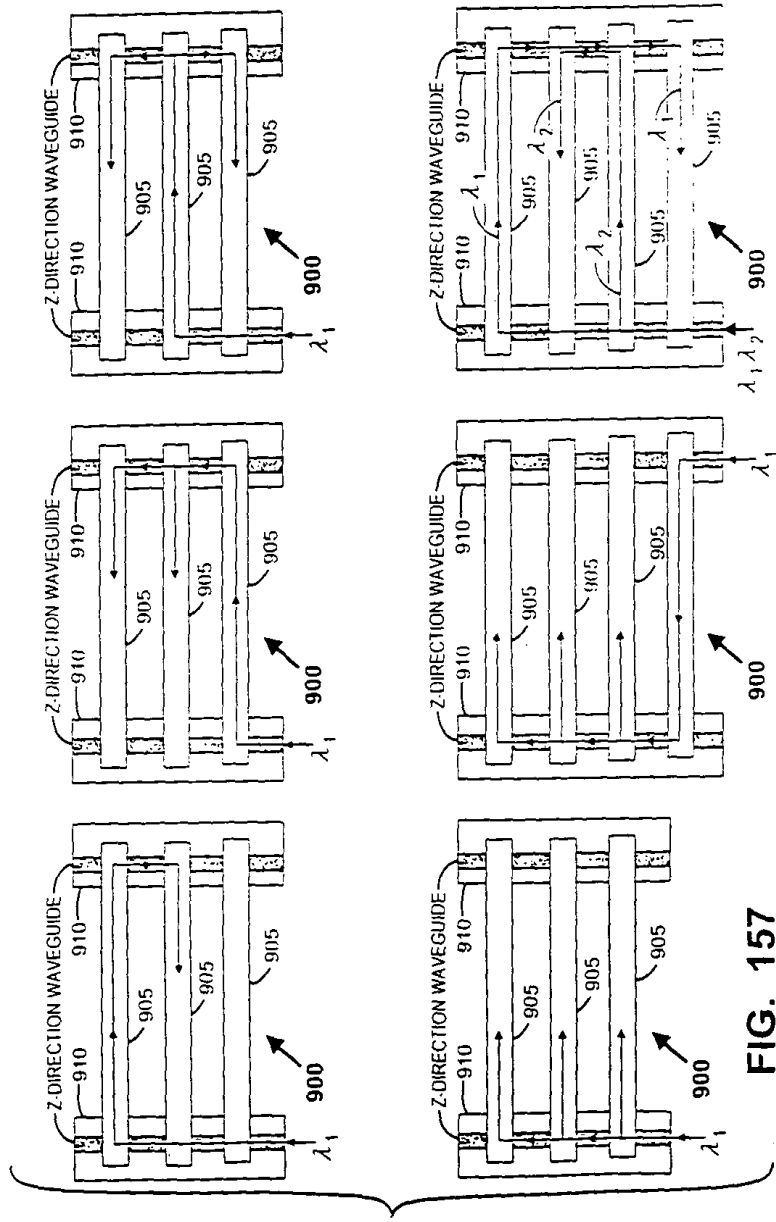


FIG. 157

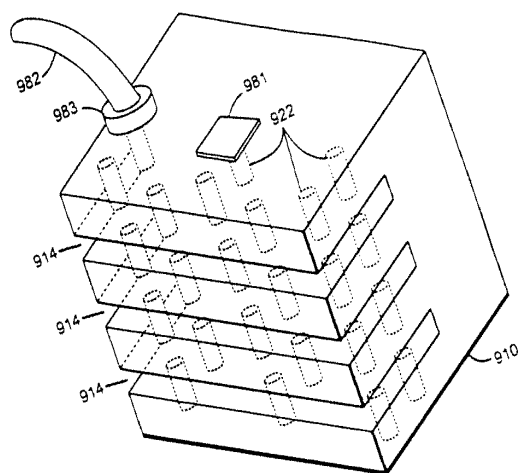


FIG. 158

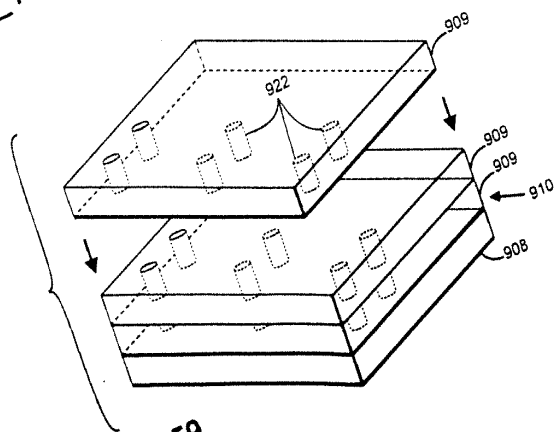


FIG. 159

204040-204040

FIG. 160

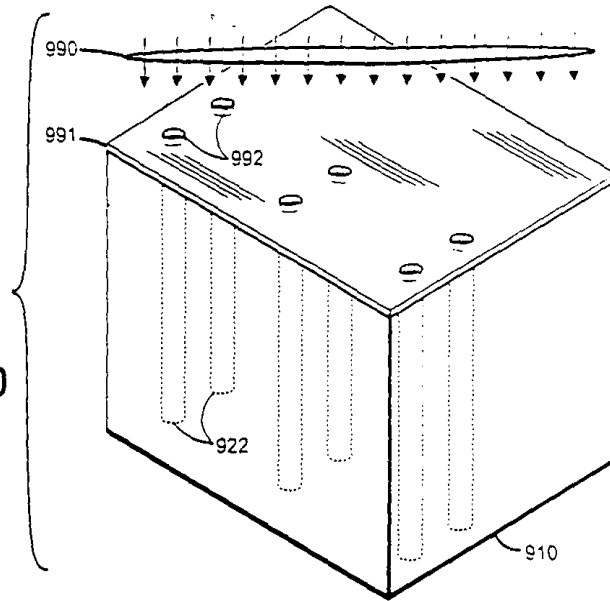
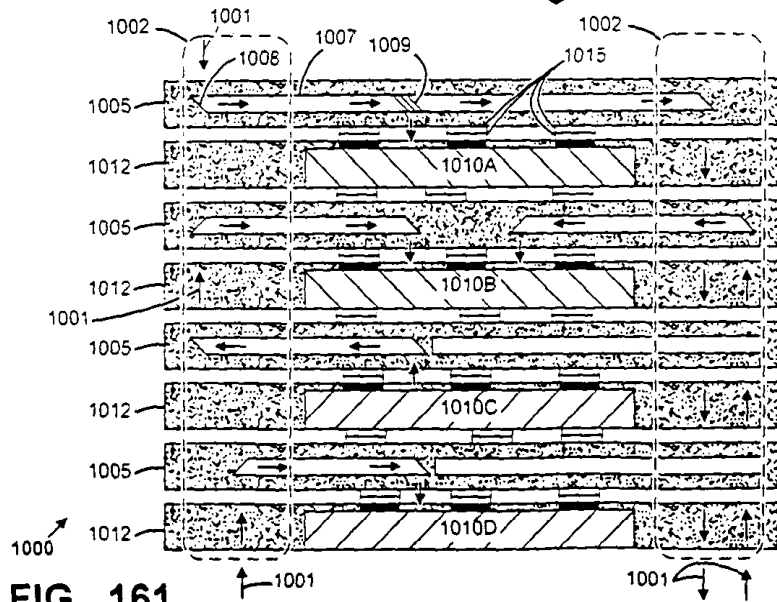
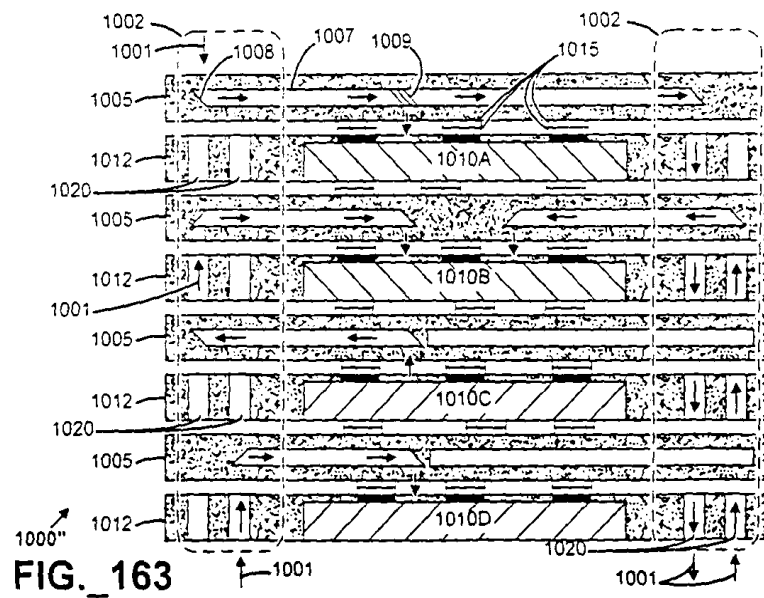
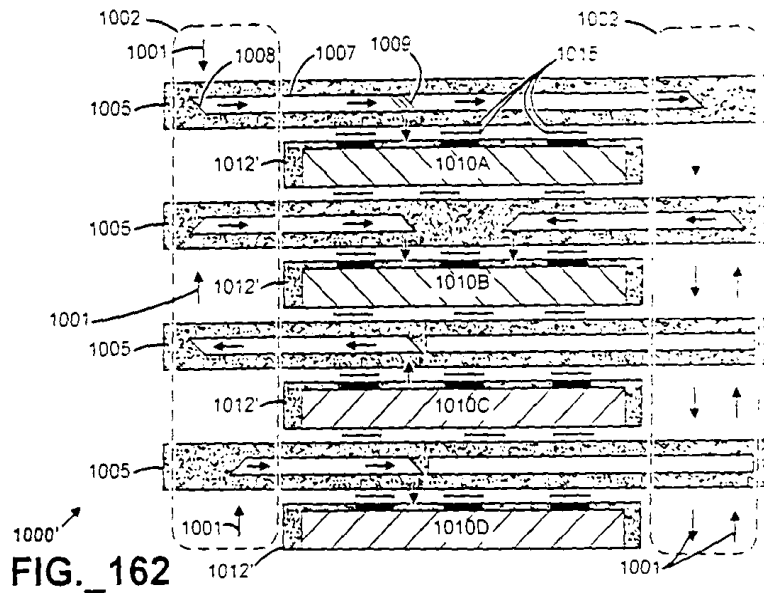
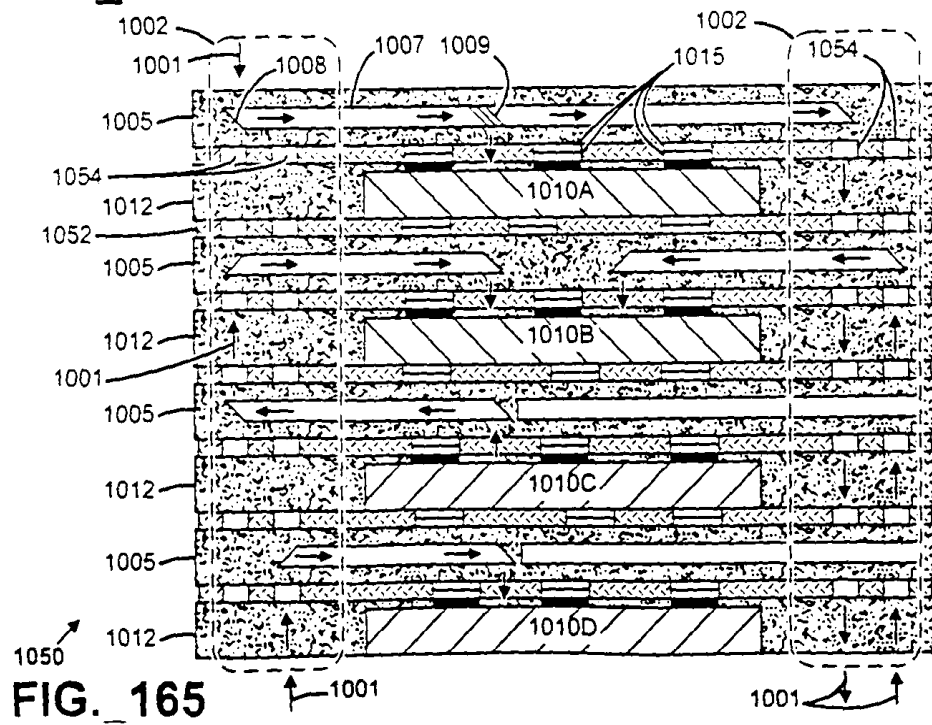
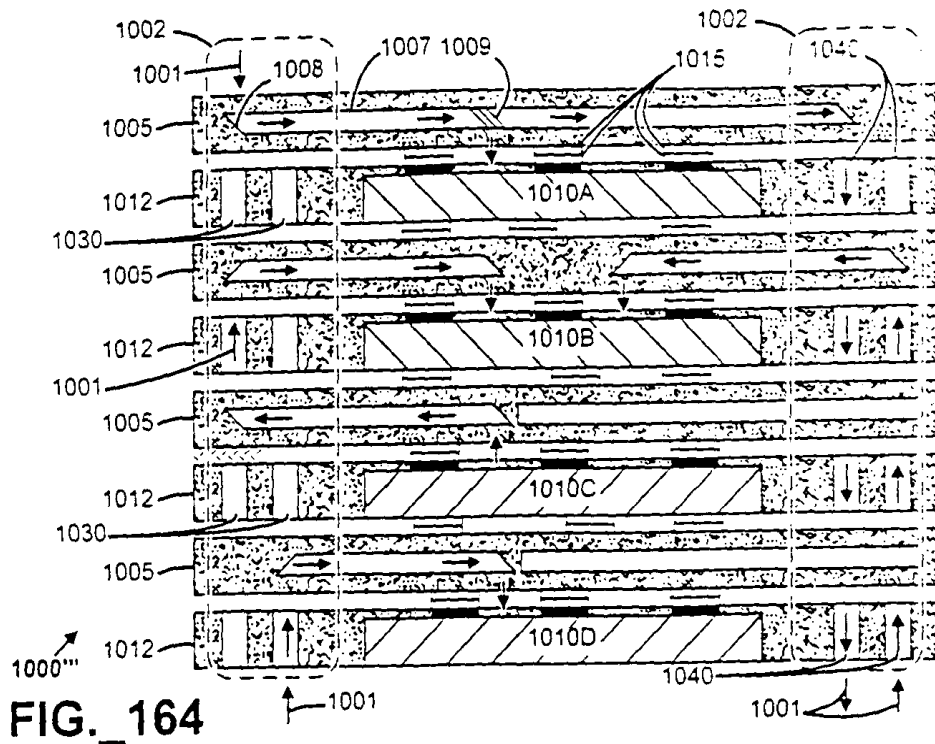
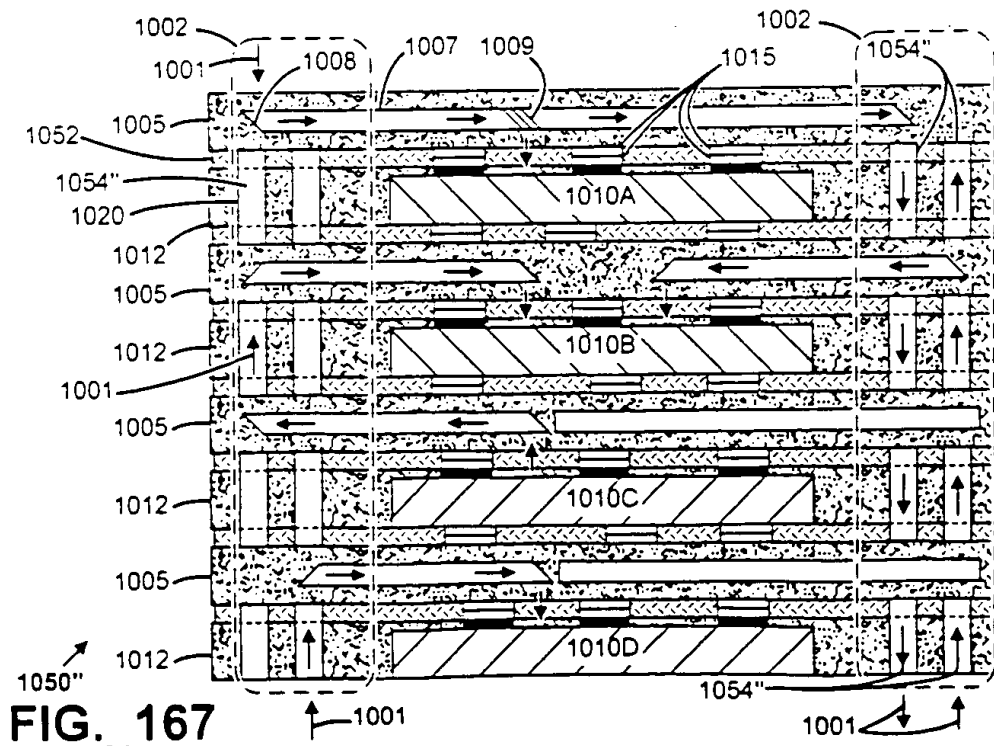
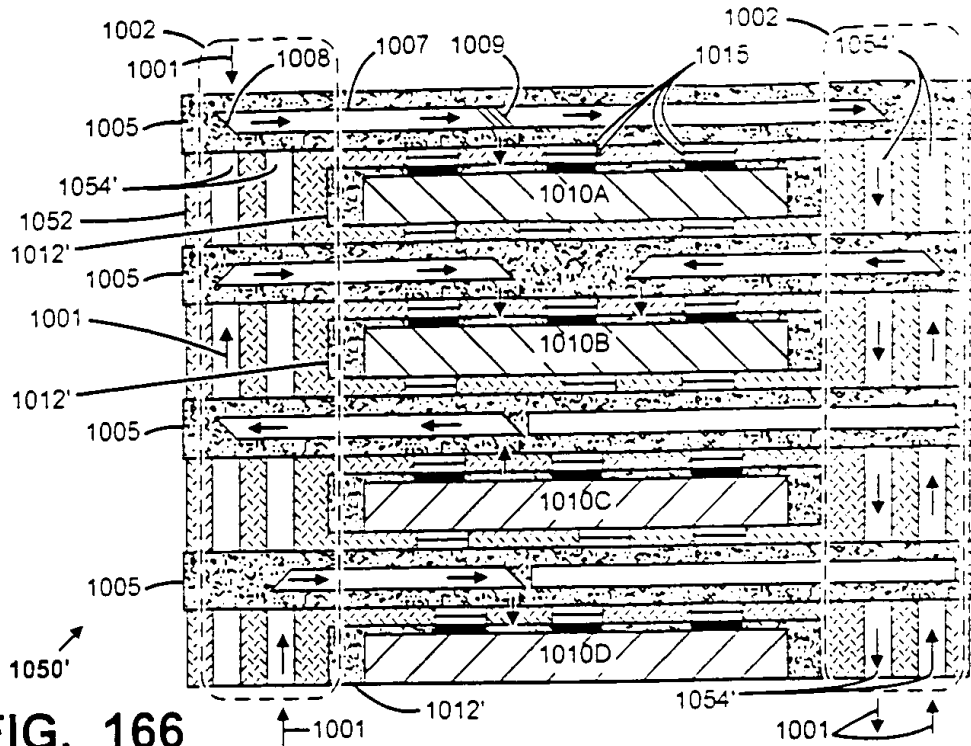


FIG. 161

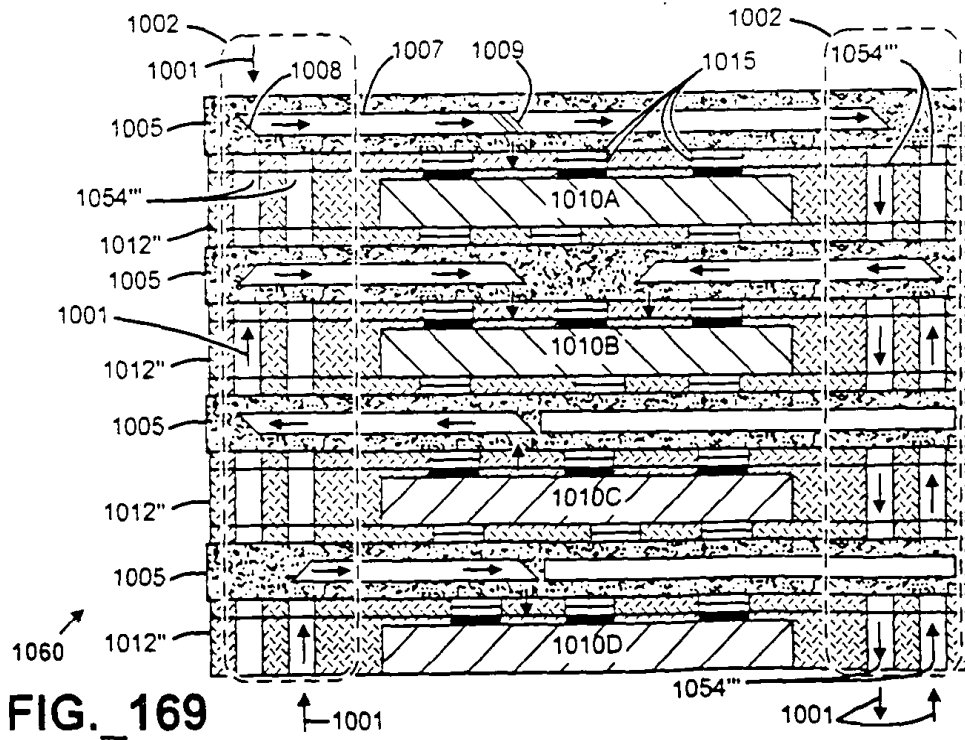
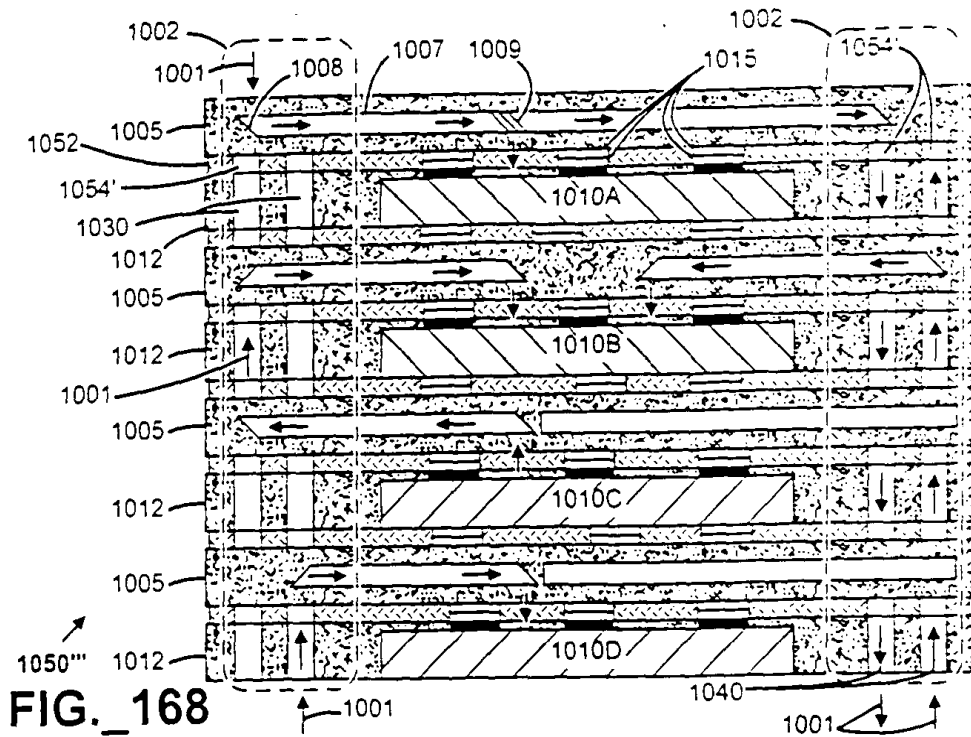








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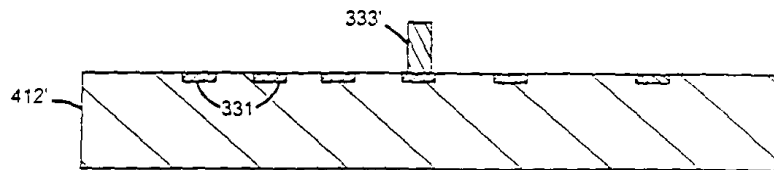


FIG.\_170

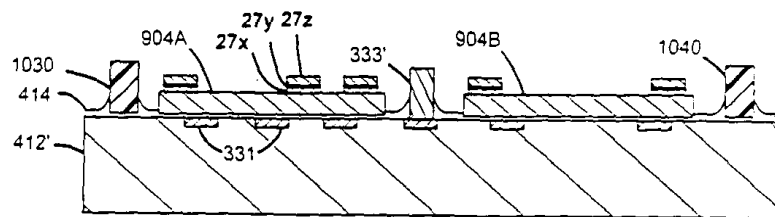


FIG.\_171

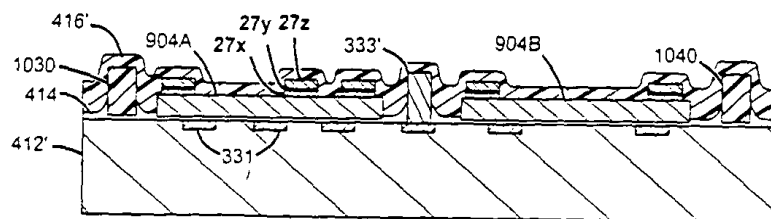


FIG.\_172

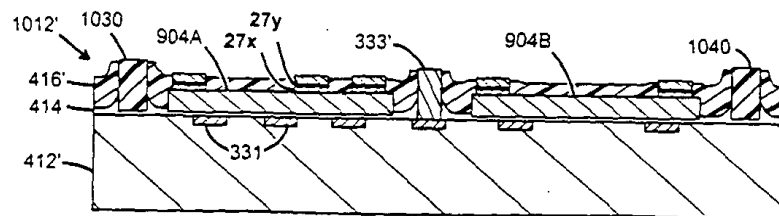


FIG.\_173



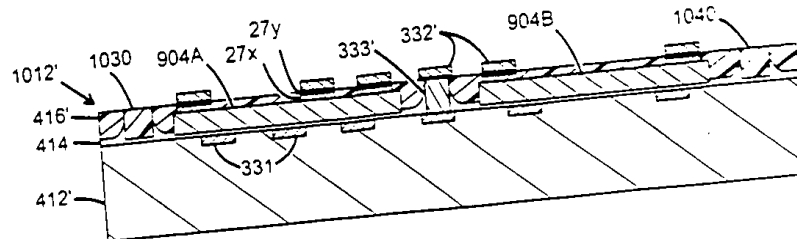


FIG. 174

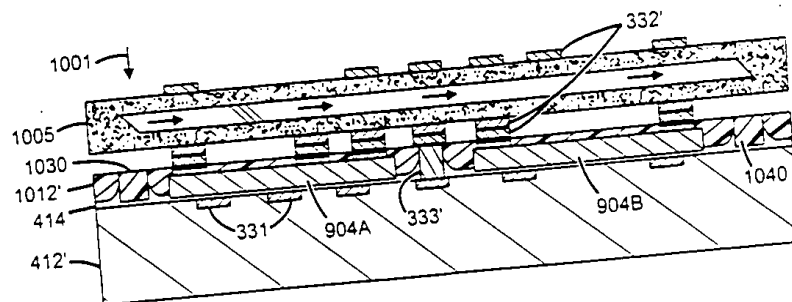


FIG. 175

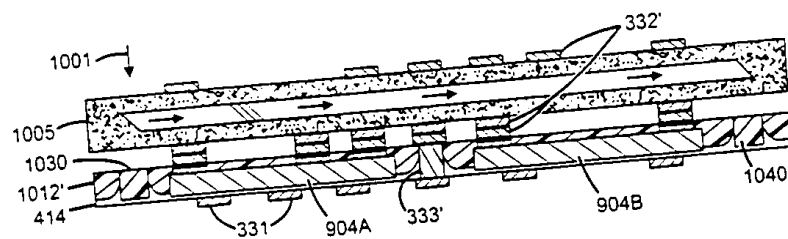
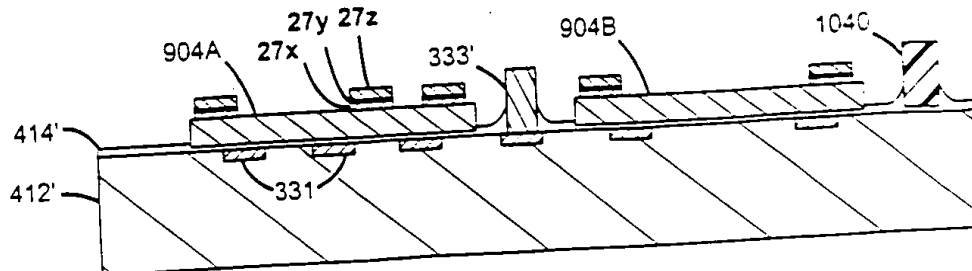
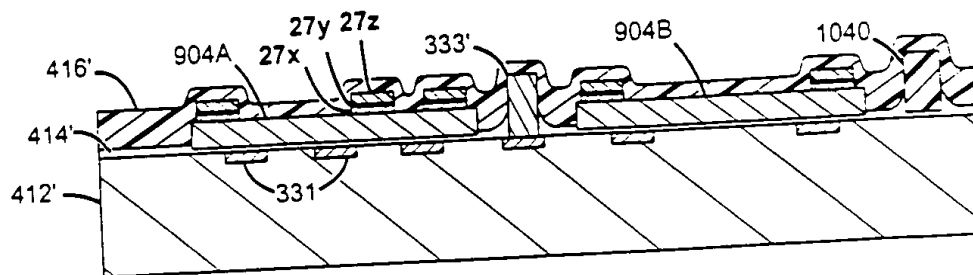


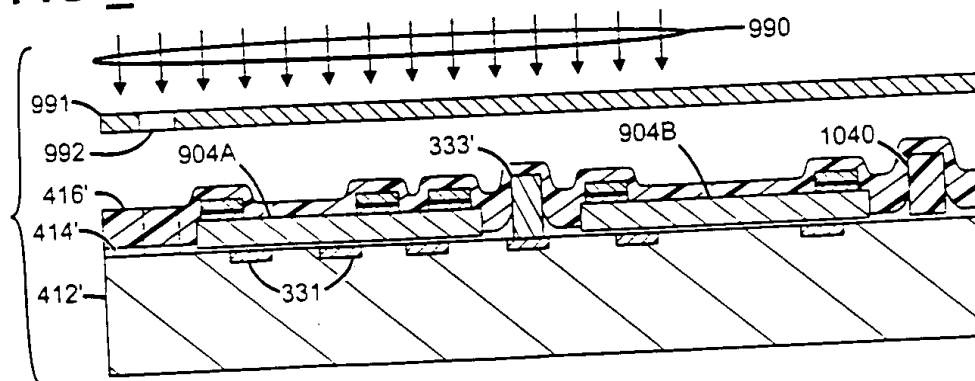
FIG. 176



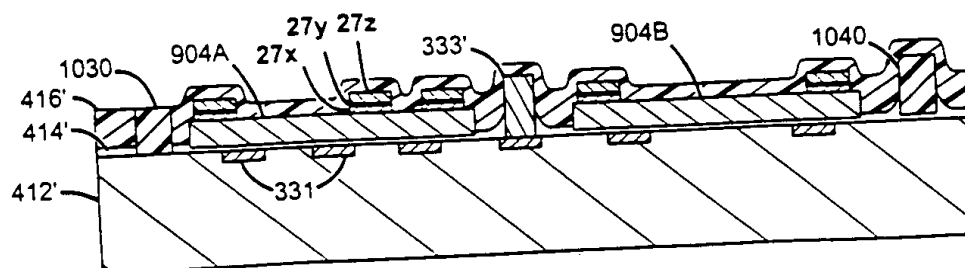
**FIG. 177**



**FIG. 178**

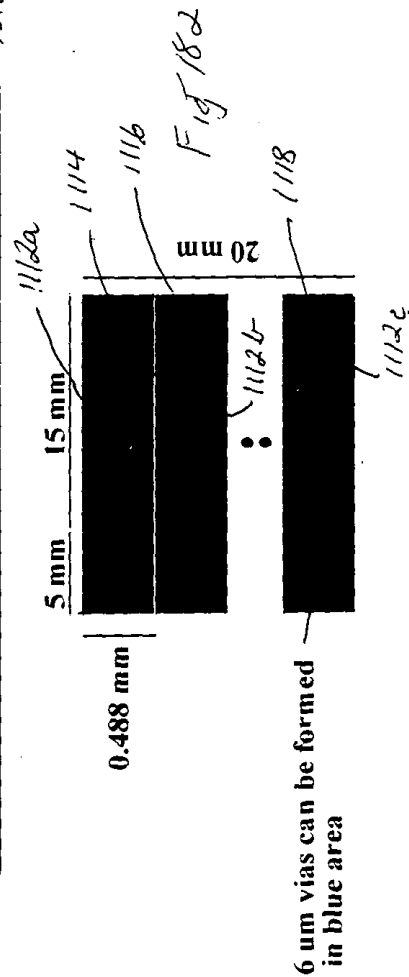
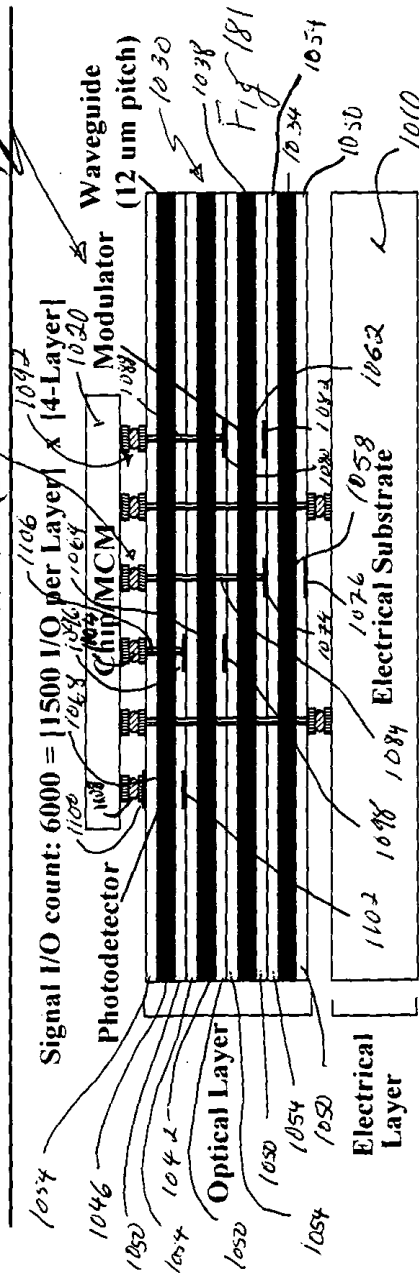


**FIG. 179**



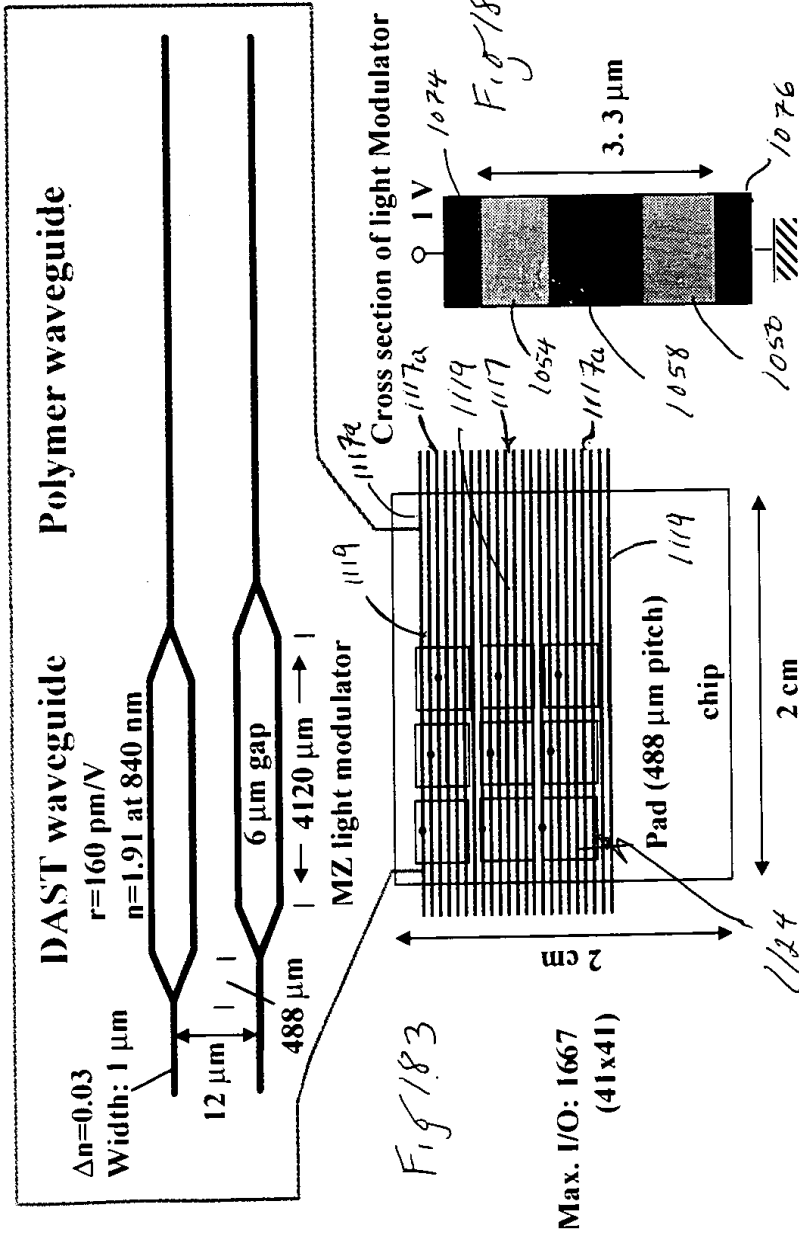
**FIG. 180**

# I/O Connection in OE Substrate (Planar Modulator)



6 um vias can be formed in blue area

FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**I/O Connection in OE Substrate (Planar Modulator)**



Max. I/O: 1667  
(41x41)

FUJITSU Computer Packaging Technologies, Inc. **FCPT**

**I/O Connection in OE Substrate (OE-VLSI)**

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

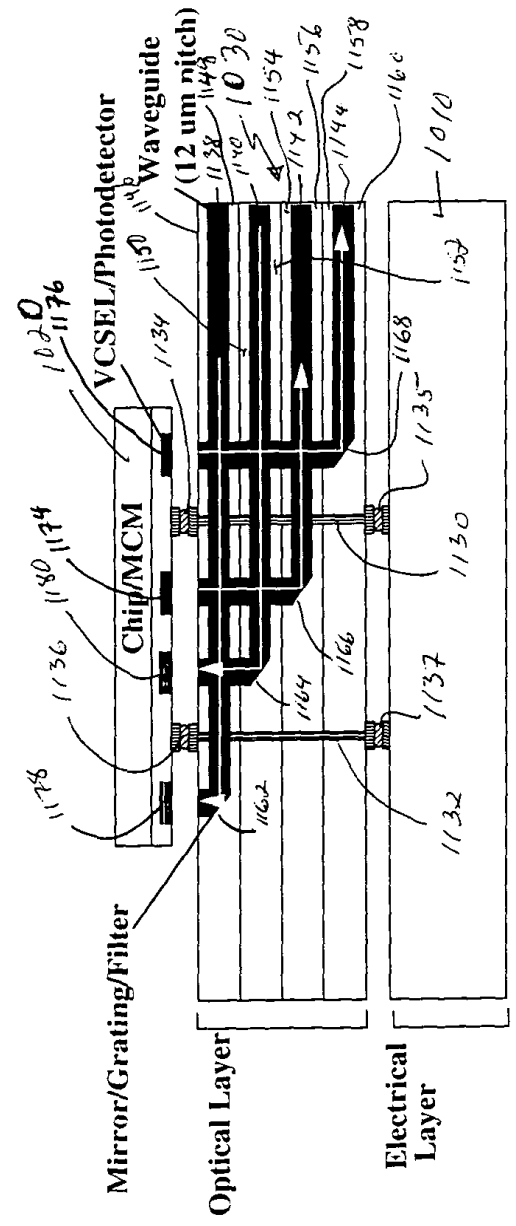
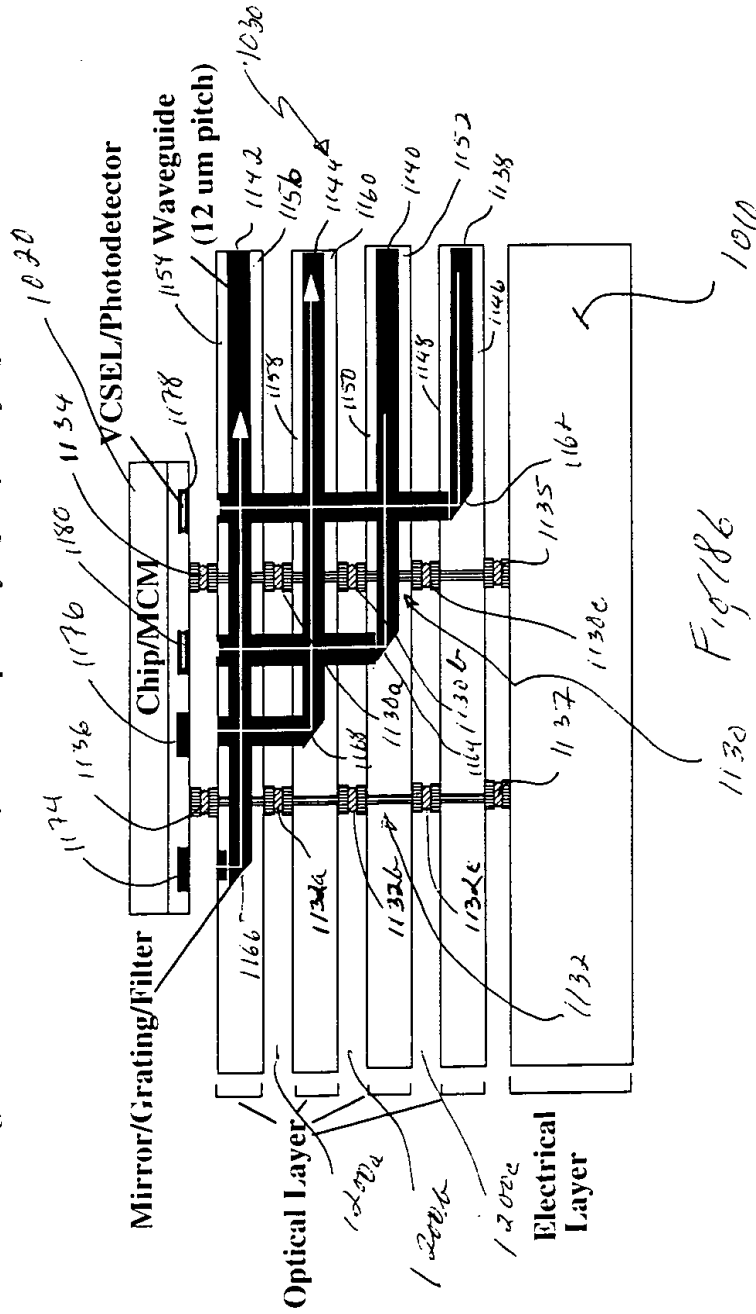


Fig 185

# I/O Connection in OE Substrate (OE-VLSI)

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]



FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**I/O Connection in OE Substrate (OE-VLSI, WDM)**

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

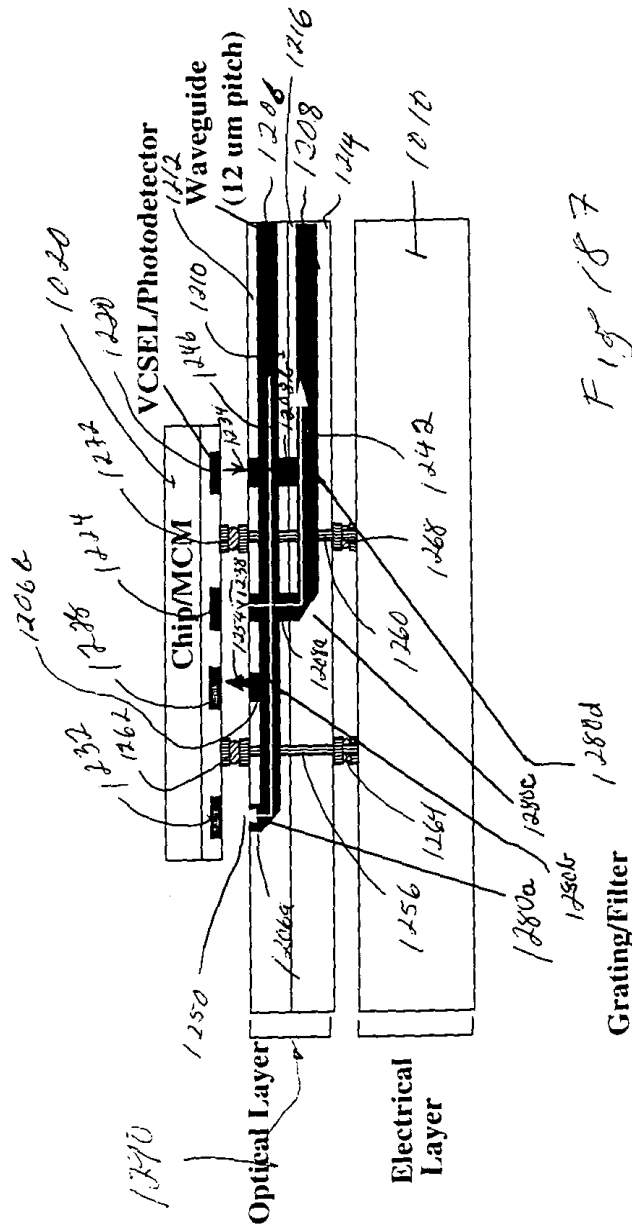


Fig 187





FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**I/O Connection in OE Substrate (Active OE Layer)**

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

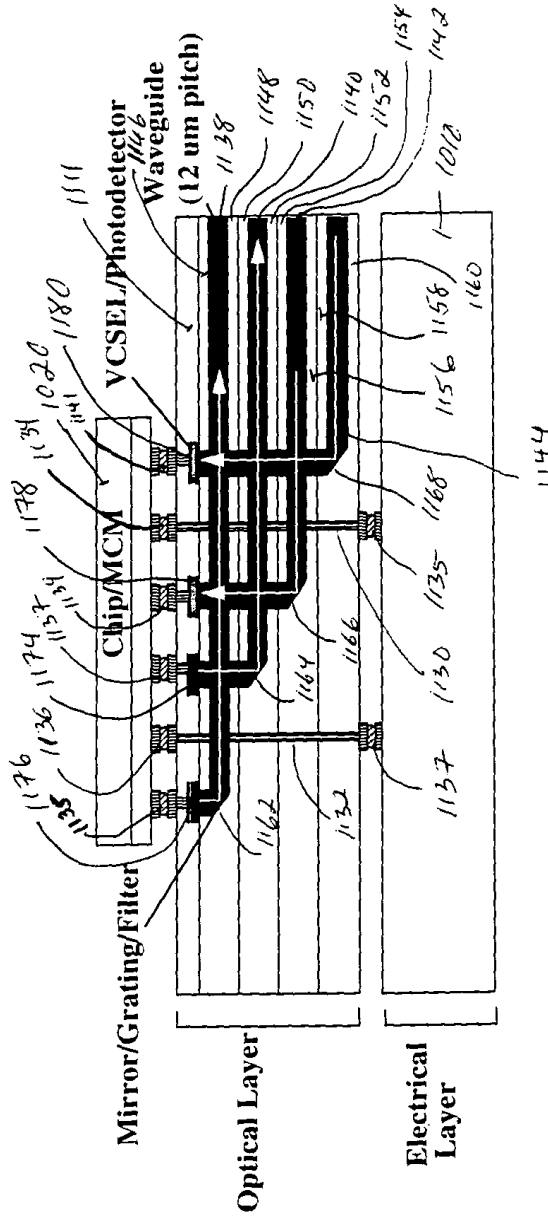


Fig 189

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

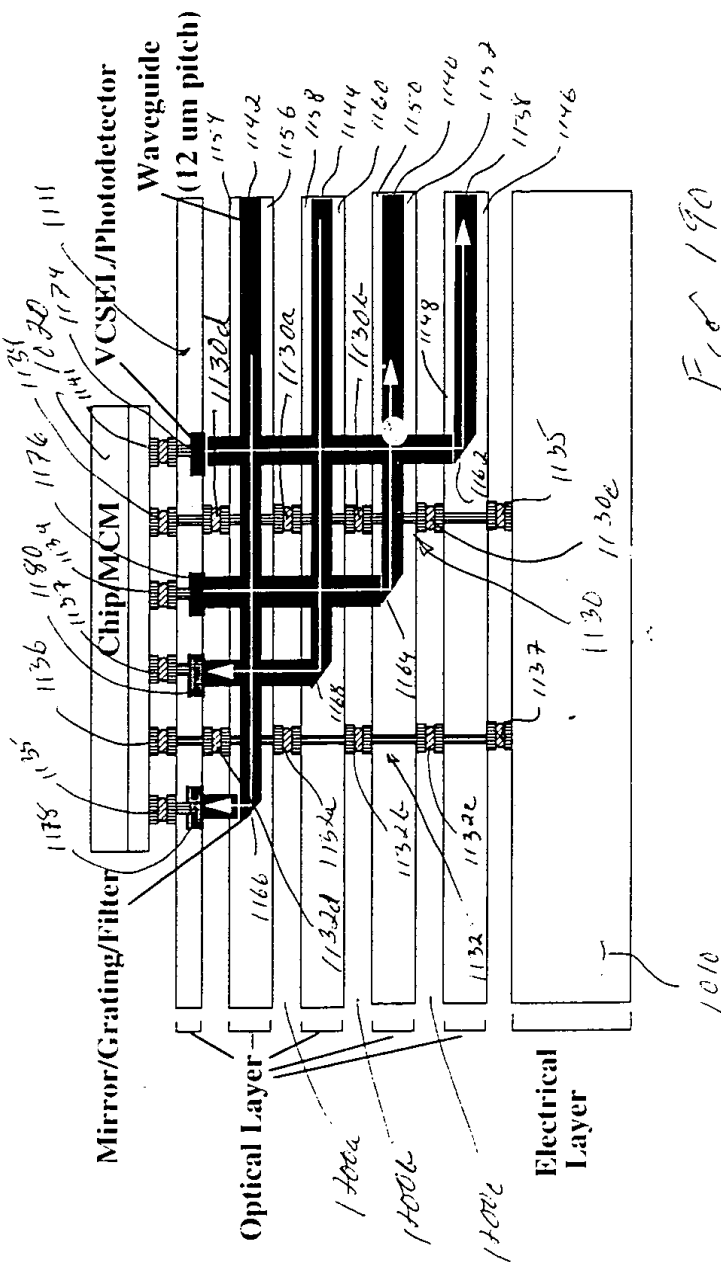


Fig 190

FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**I/O Connection in OE Substrate (Active OE Layer, WDM)**

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

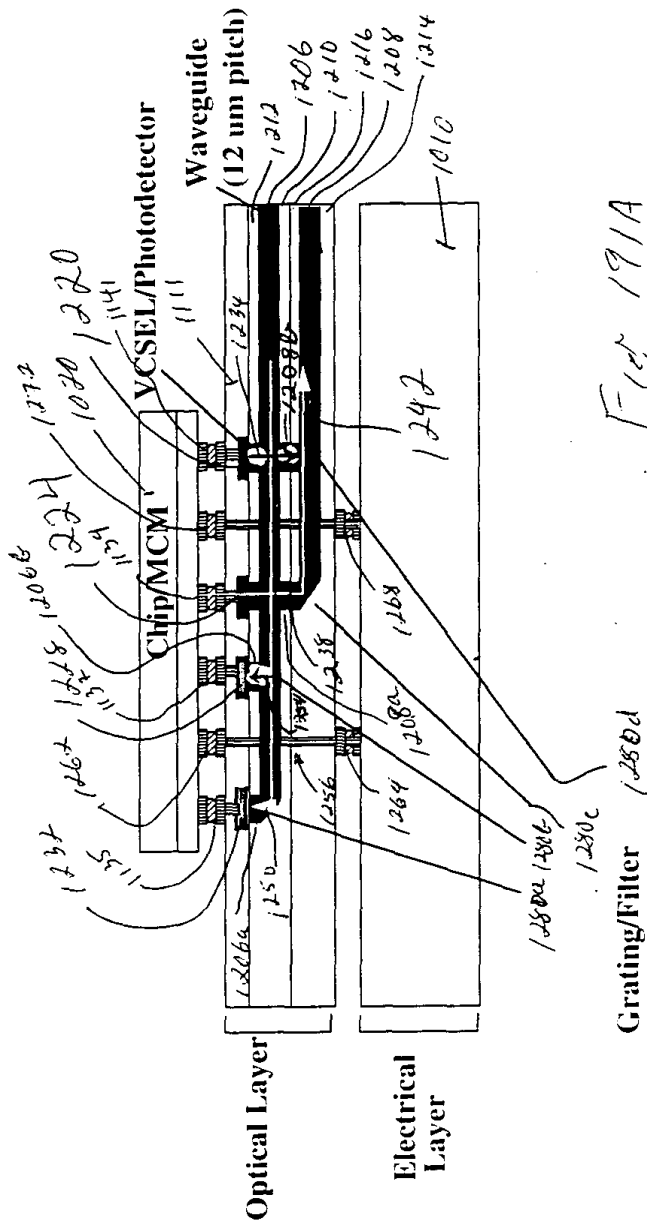


Fig 191A

FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**I/O Connection in OE Substrate (Active OE Layer, WDM)**

Signal I/O count: 6000 = [1500 I/O per Layer] x [4-Layer]

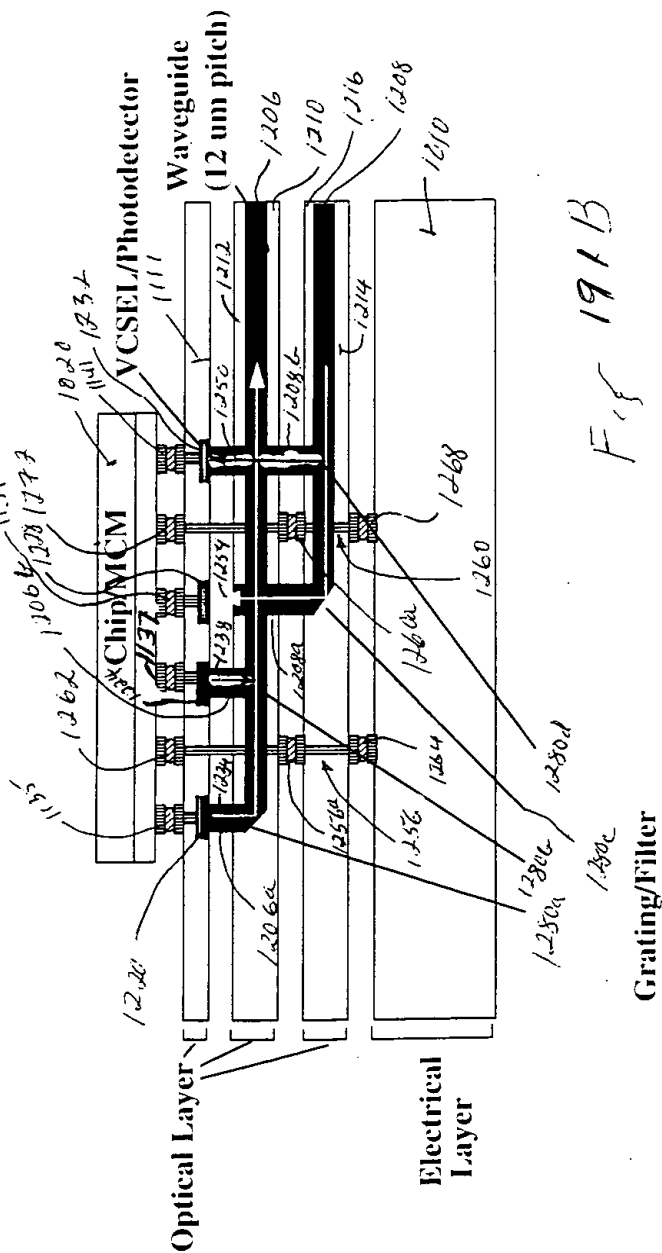
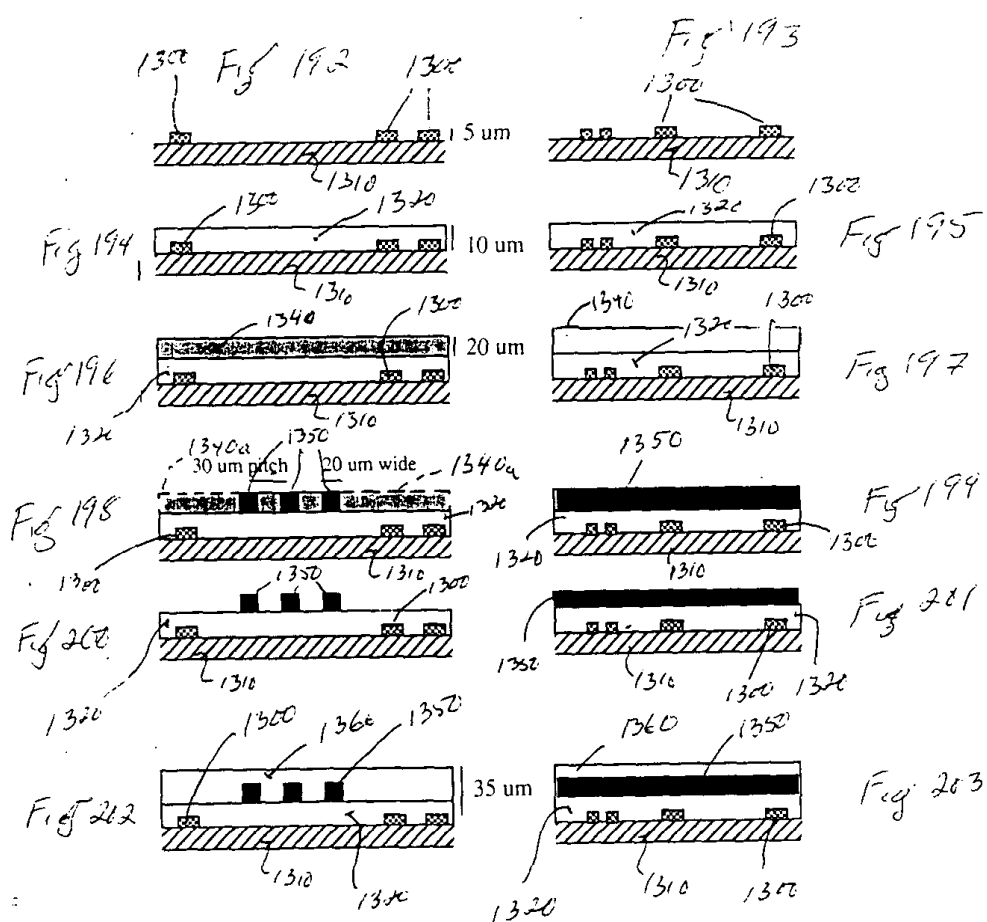
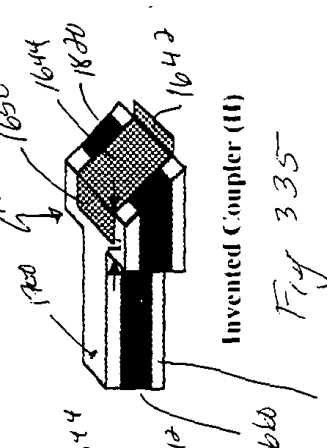
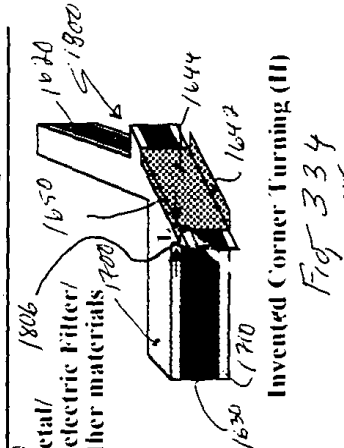
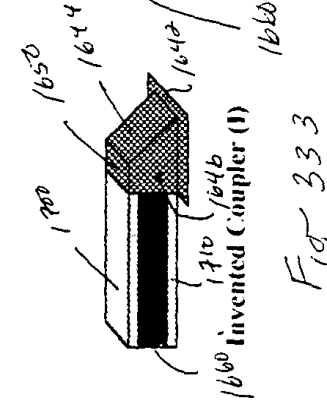
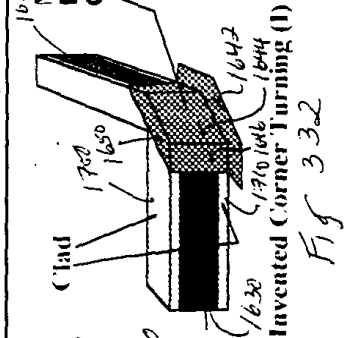
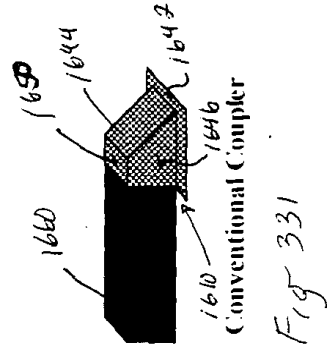
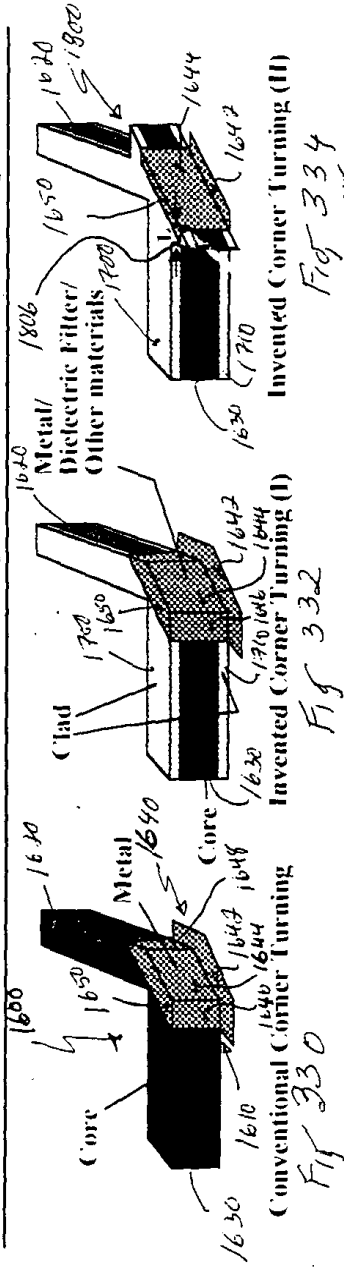


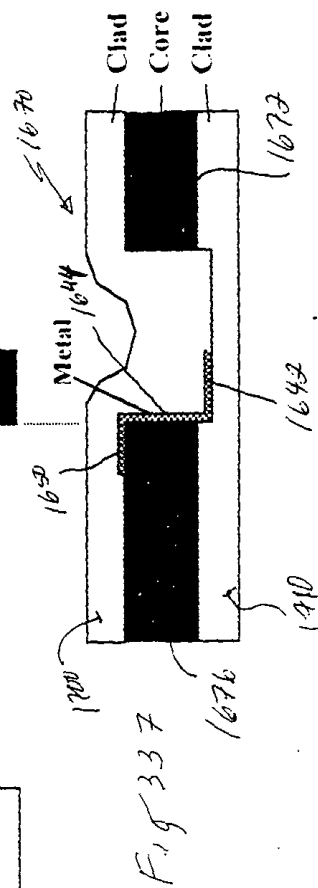
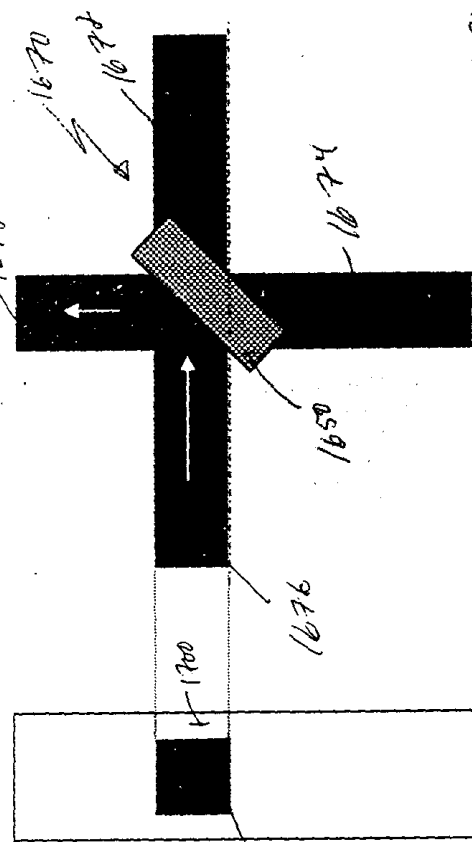
Fig 191B



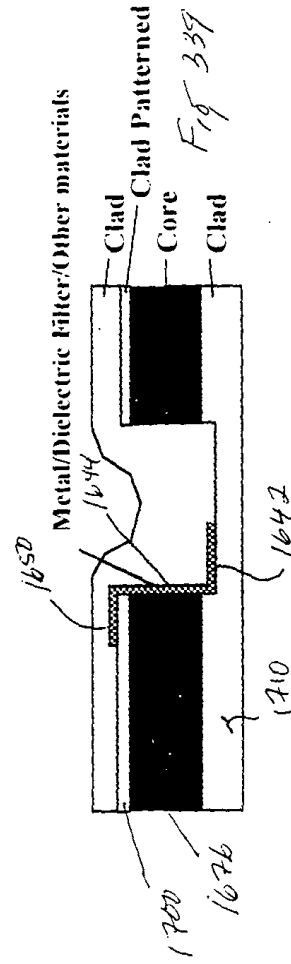
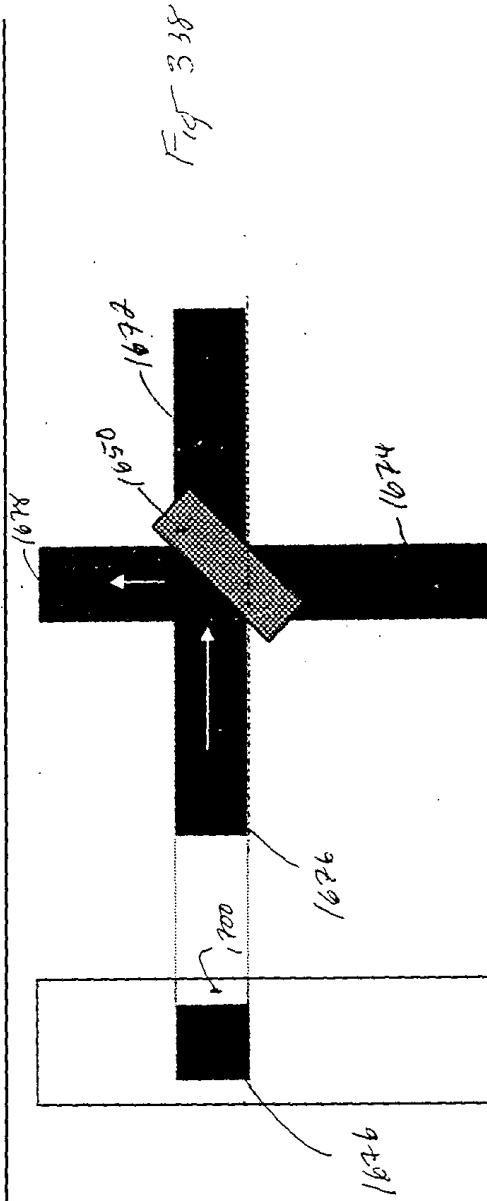
# Conventional and Invented Waveguide Structure Examples



## Conventional Corner Turning Structure

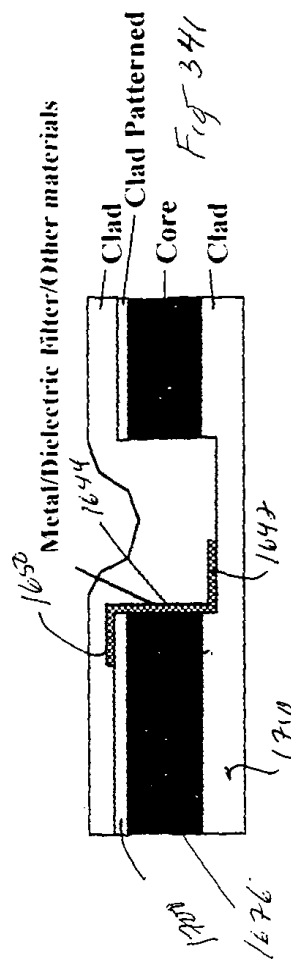
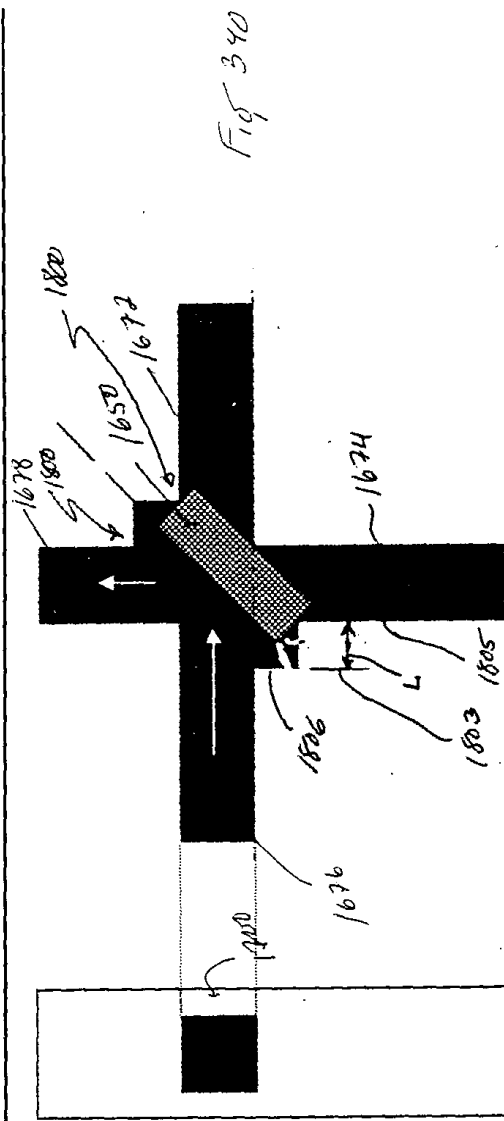


# **Invented Corner Turning Structure (I)**

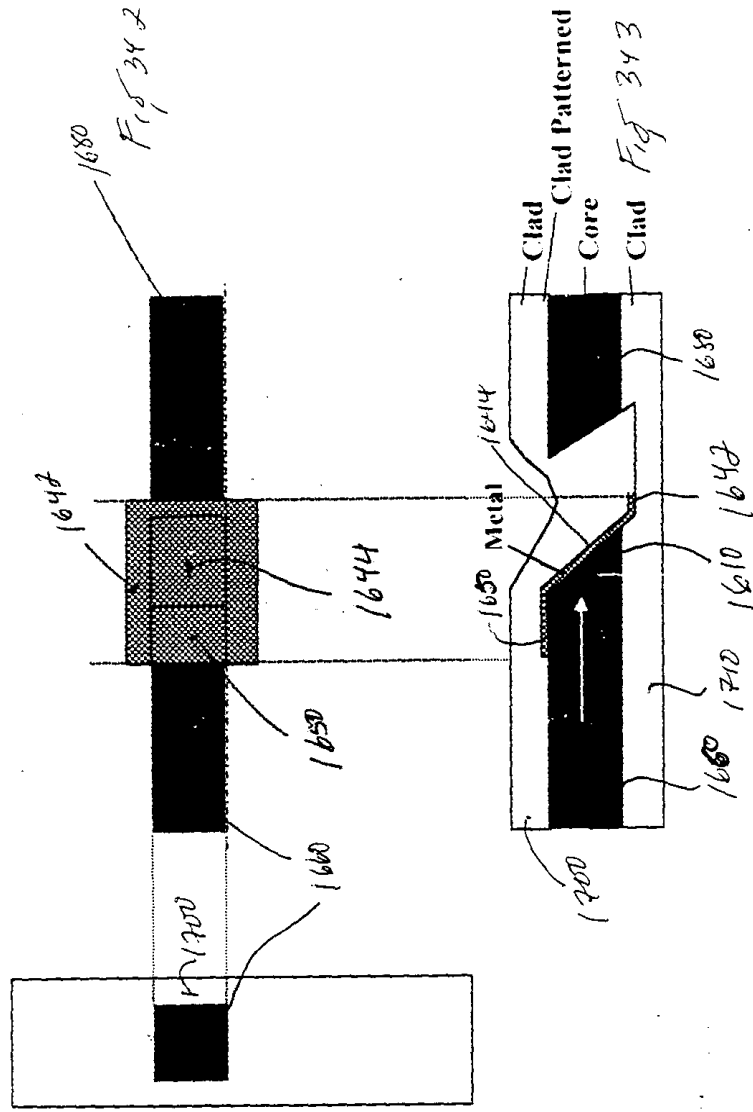




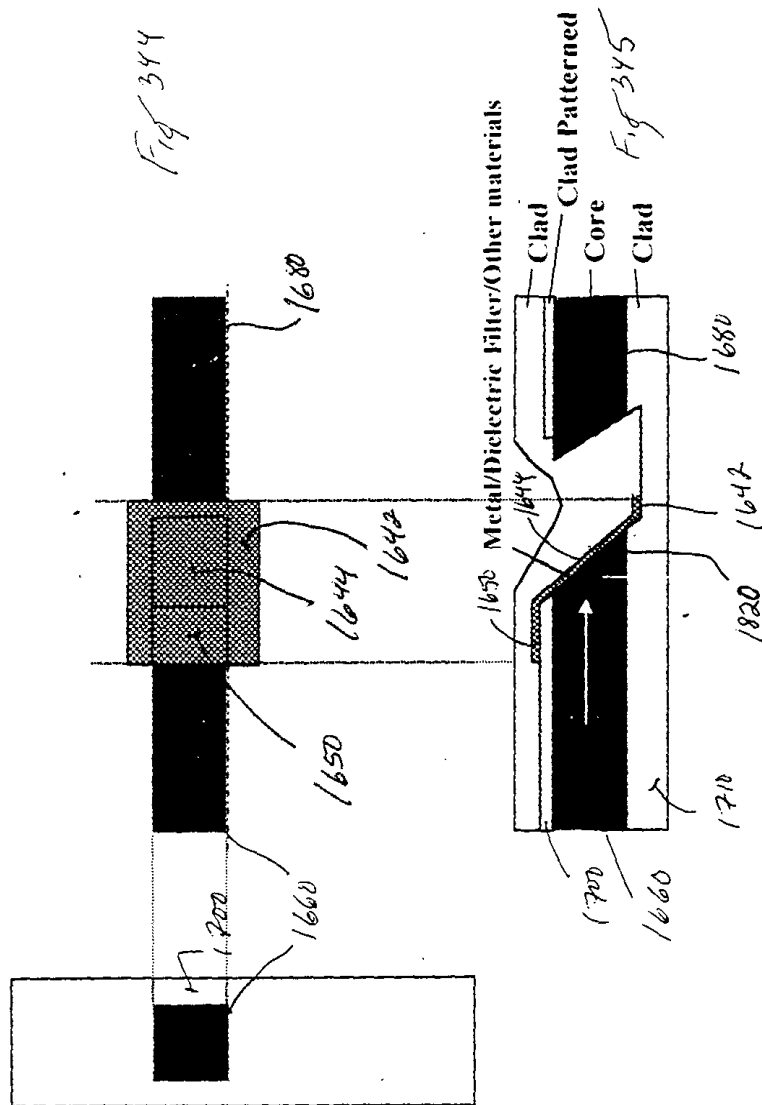
## Invented Corner Turning Structure (II)

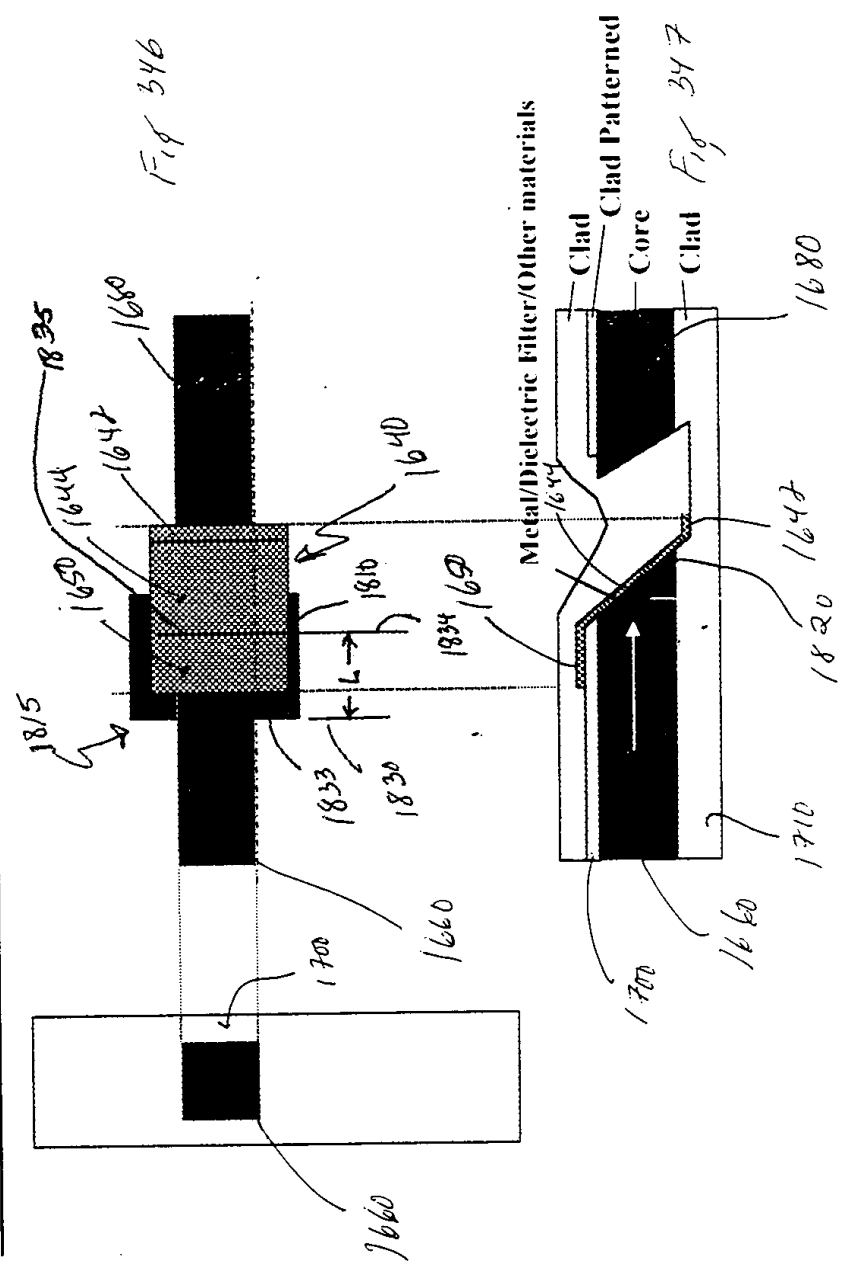


# Conventional Coupler Structure (I)

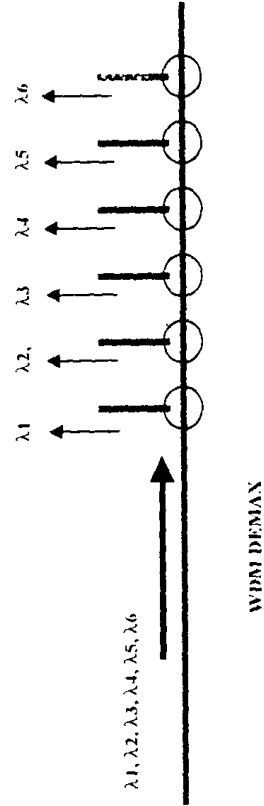
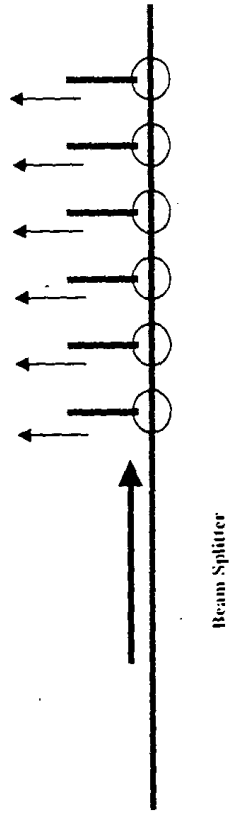


# Invented Coupler Structure (I)



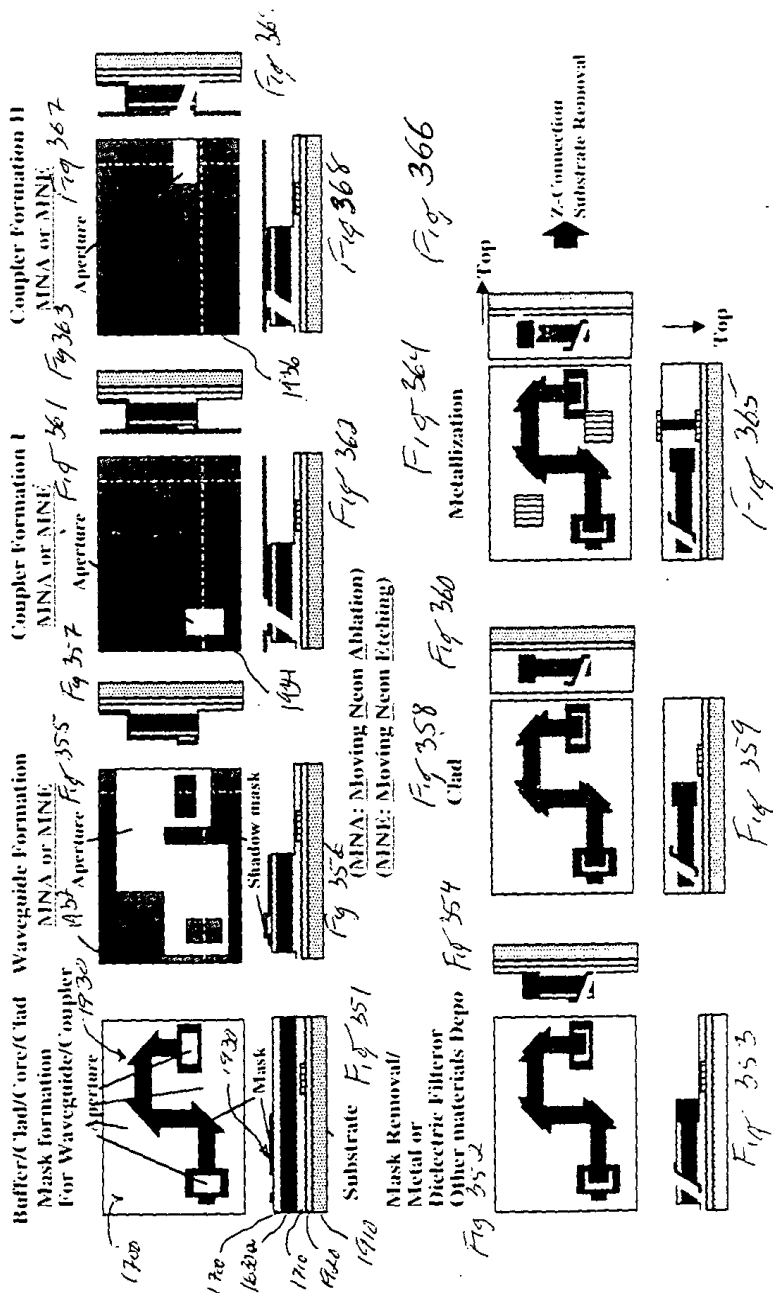


FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**Excimer Laser Ablation Example for Beveled Cut (2)**

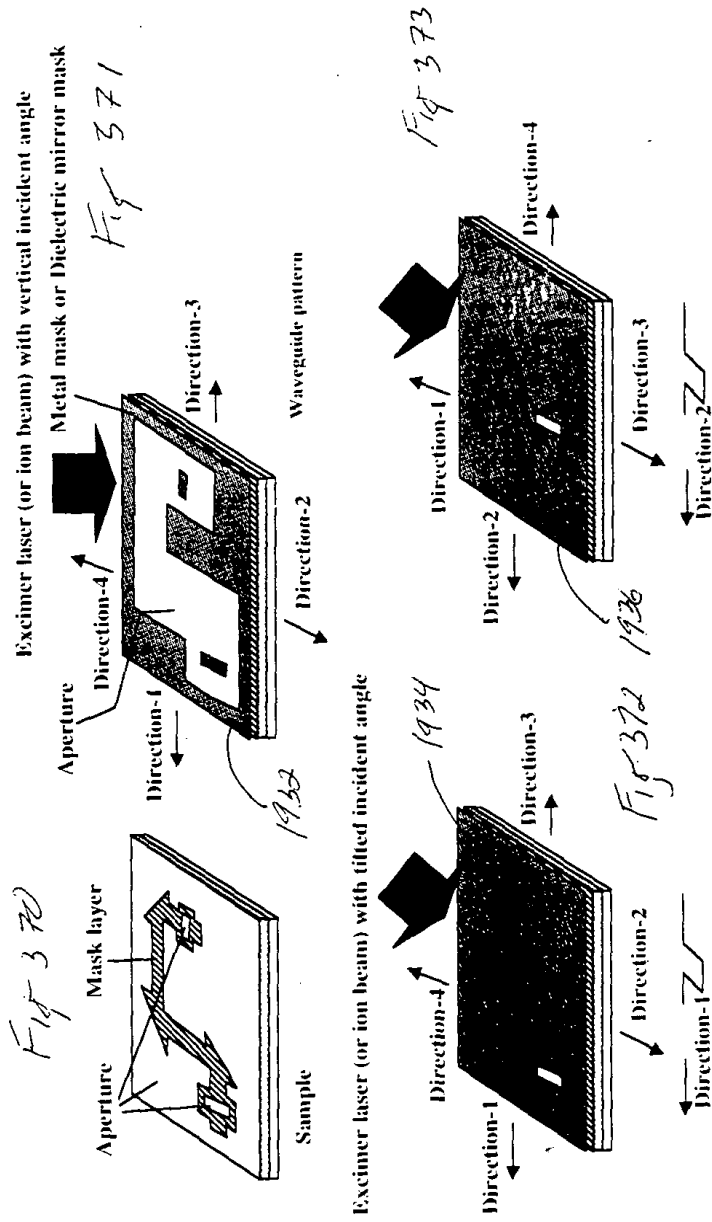


# Another Process Flow for Structure (II)

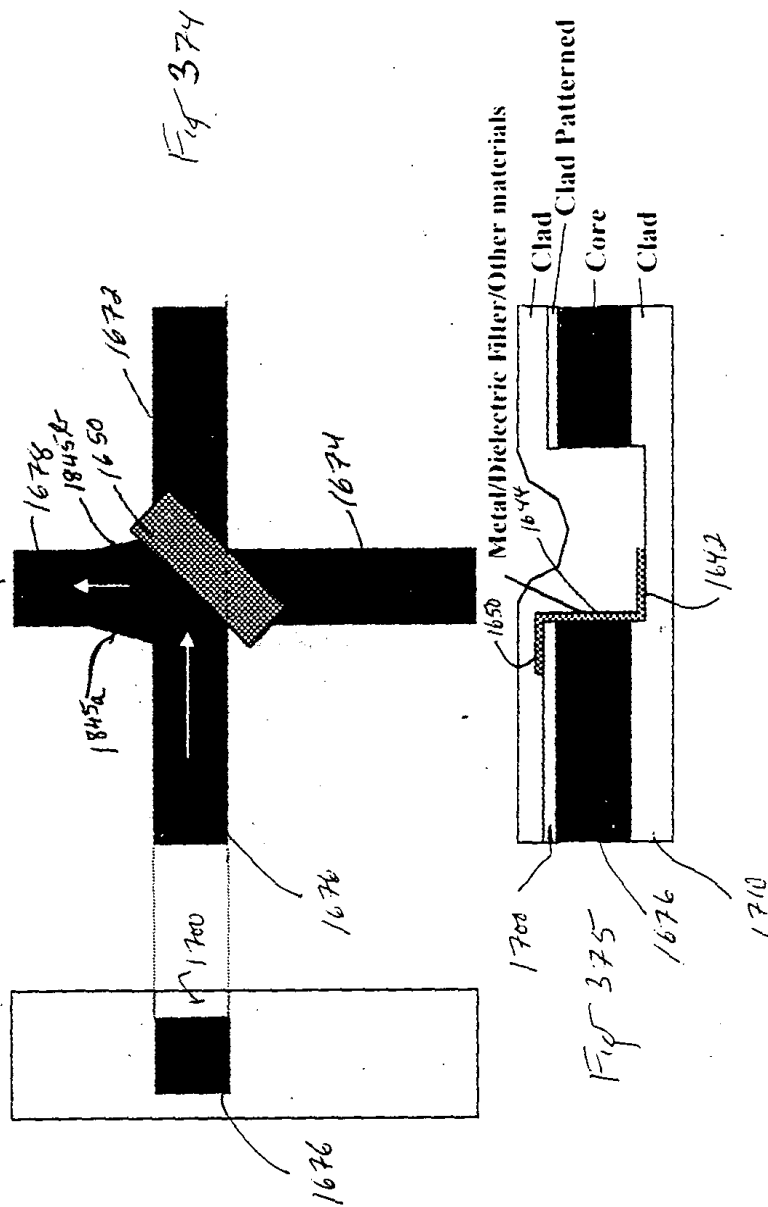
Fig 350



FUJITSU Computer Packaging Technologies, Inc. **FCPT**  
**MNA, MNE Example for Add2 example**

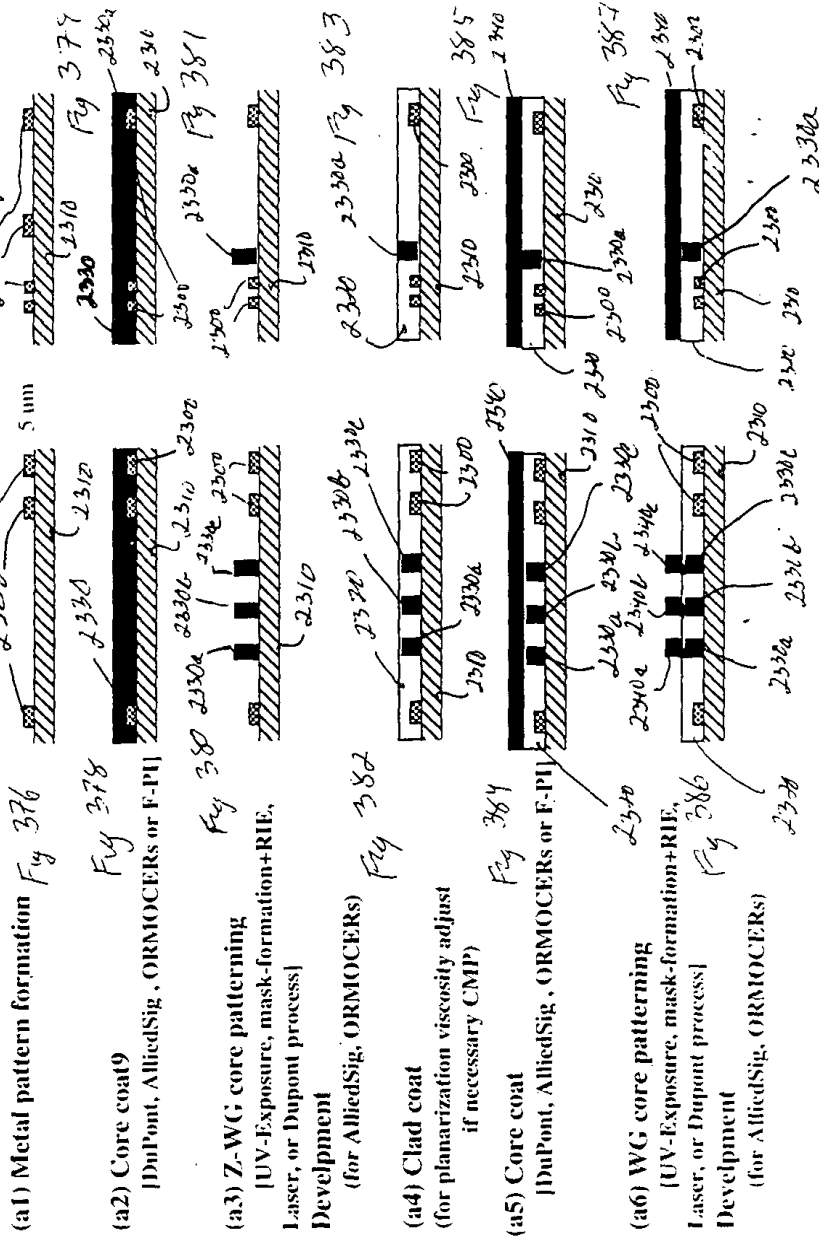


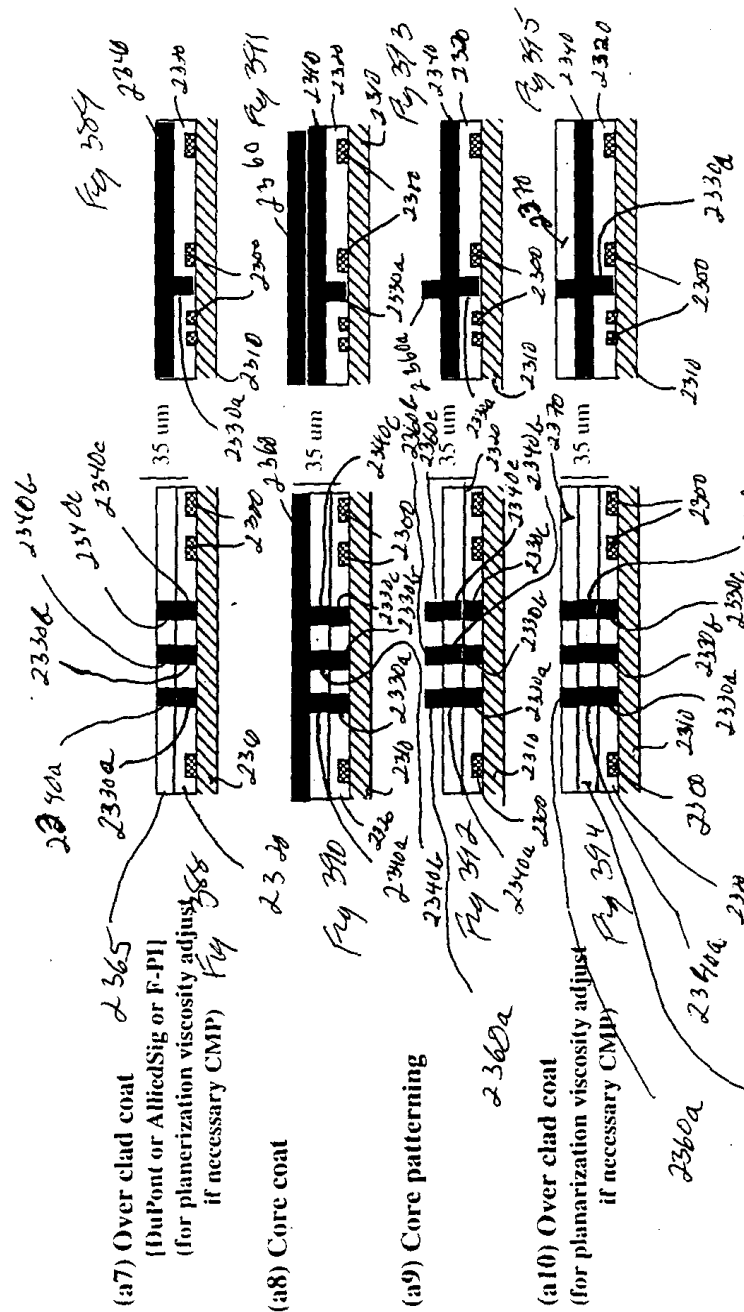
### Invented Corner Turning Structure (A)





### Example 3: Z waveguide Fab. Process 1

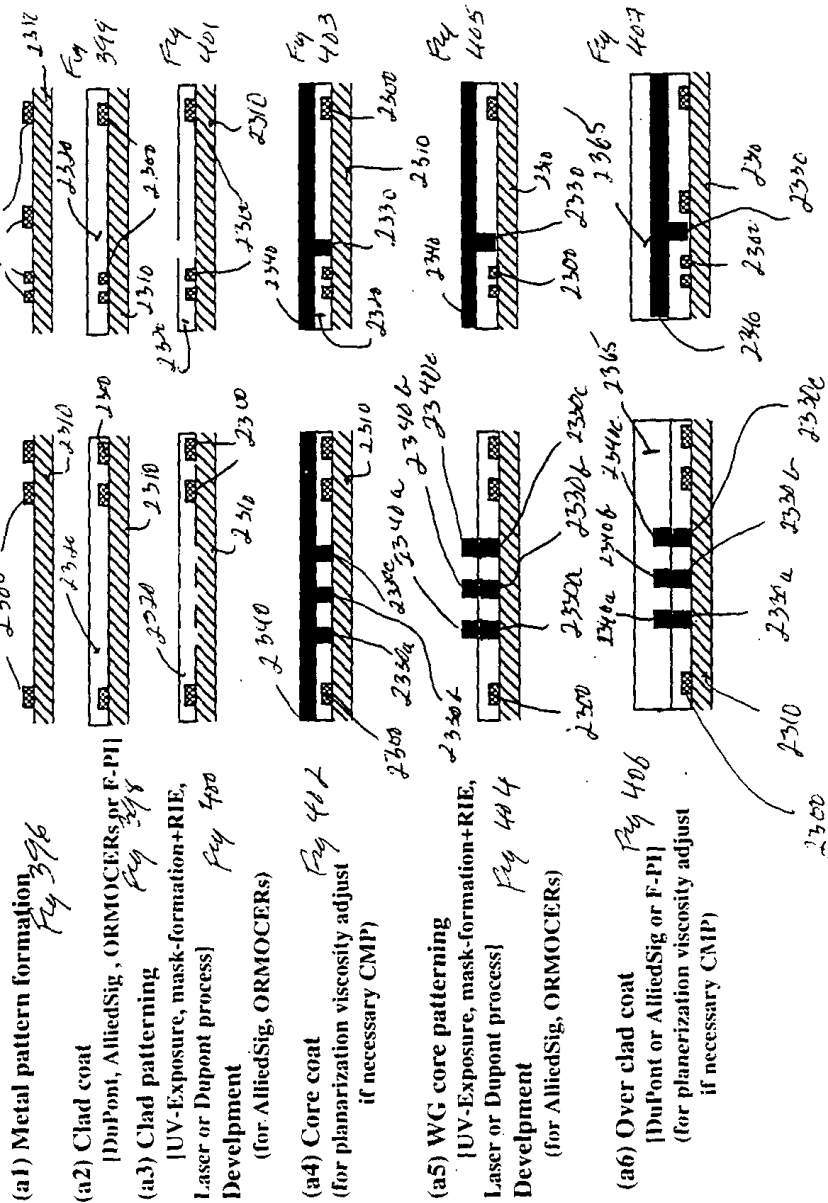


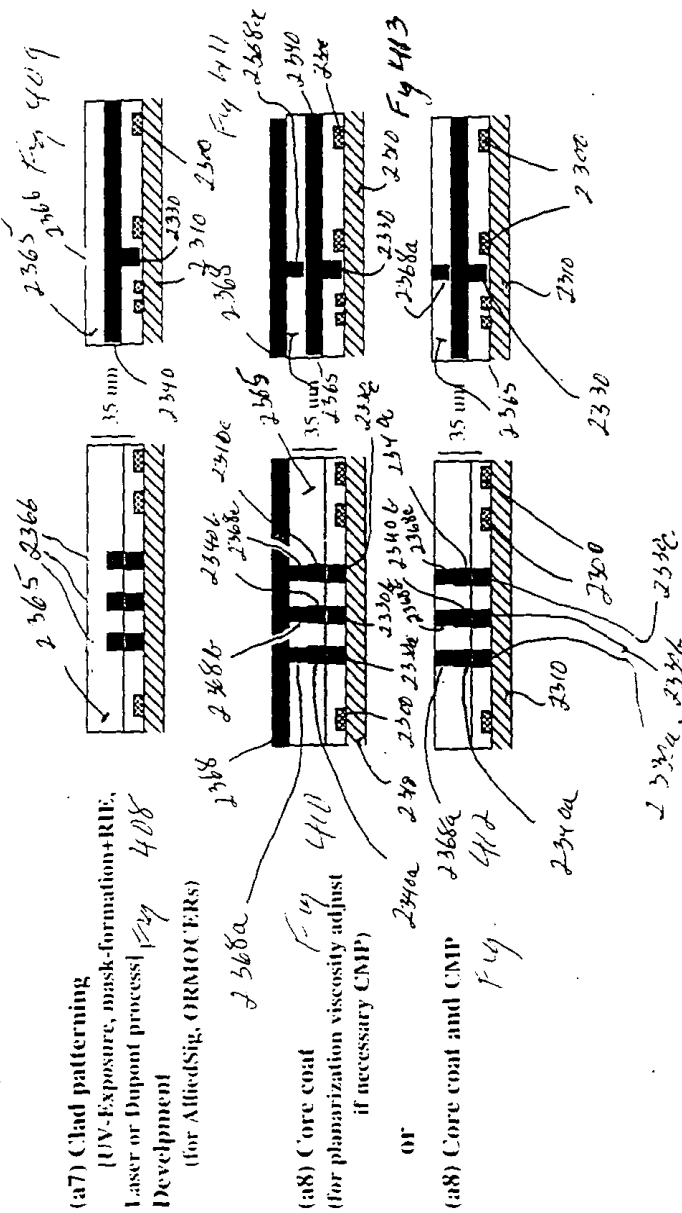


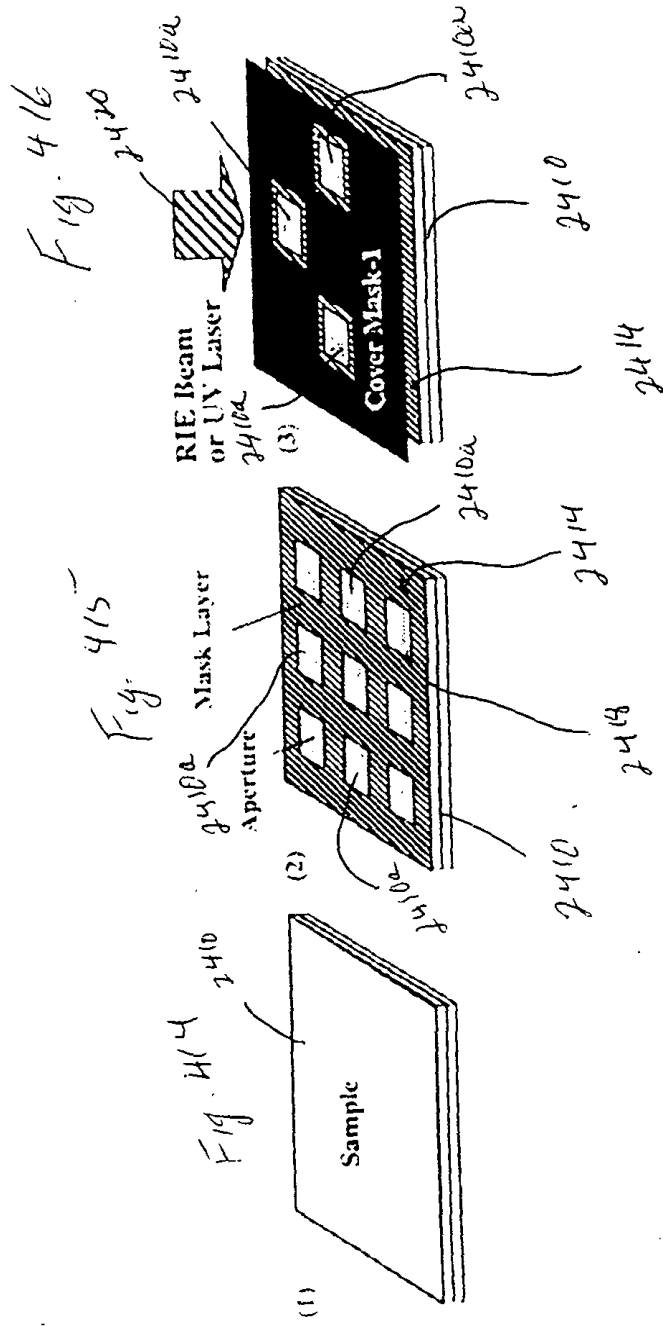
In the case of multi layer (a1-a10) or (a2-a10) process is repeated on the (a10).

## Example 4: Z waveguide Fab. Process 2

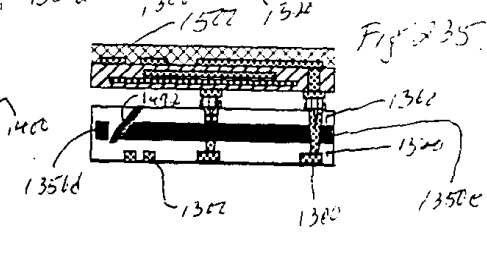
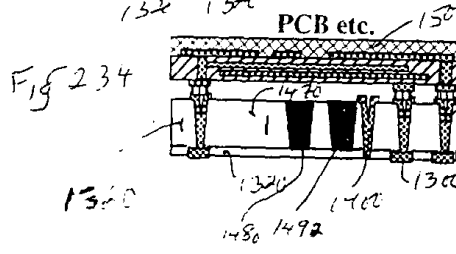
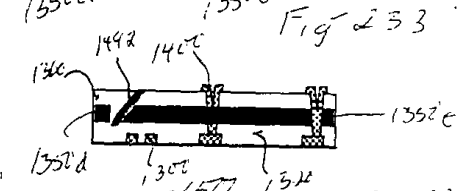
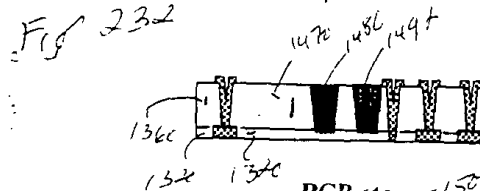
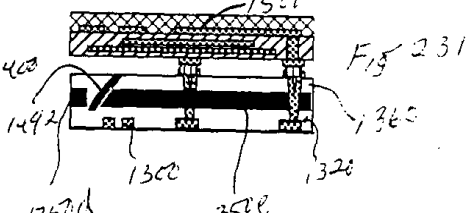
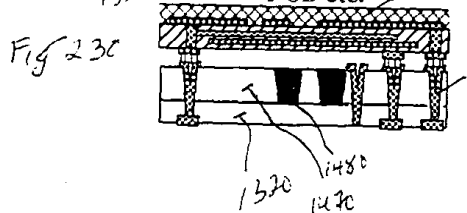
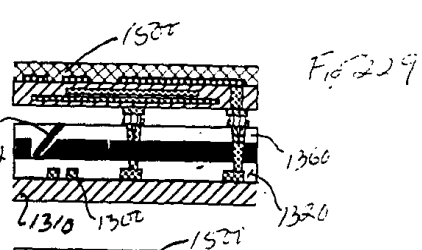
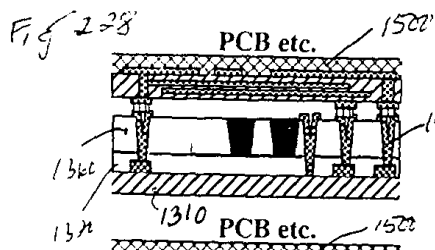
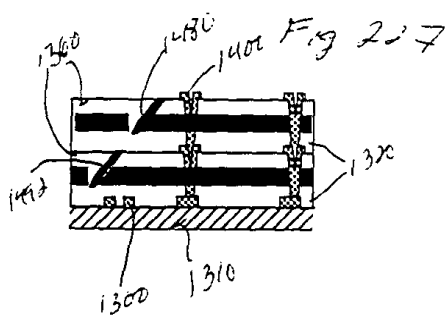
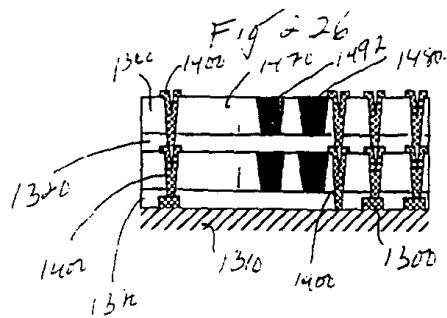
Fig 397















[illegible]

20140401 28579260

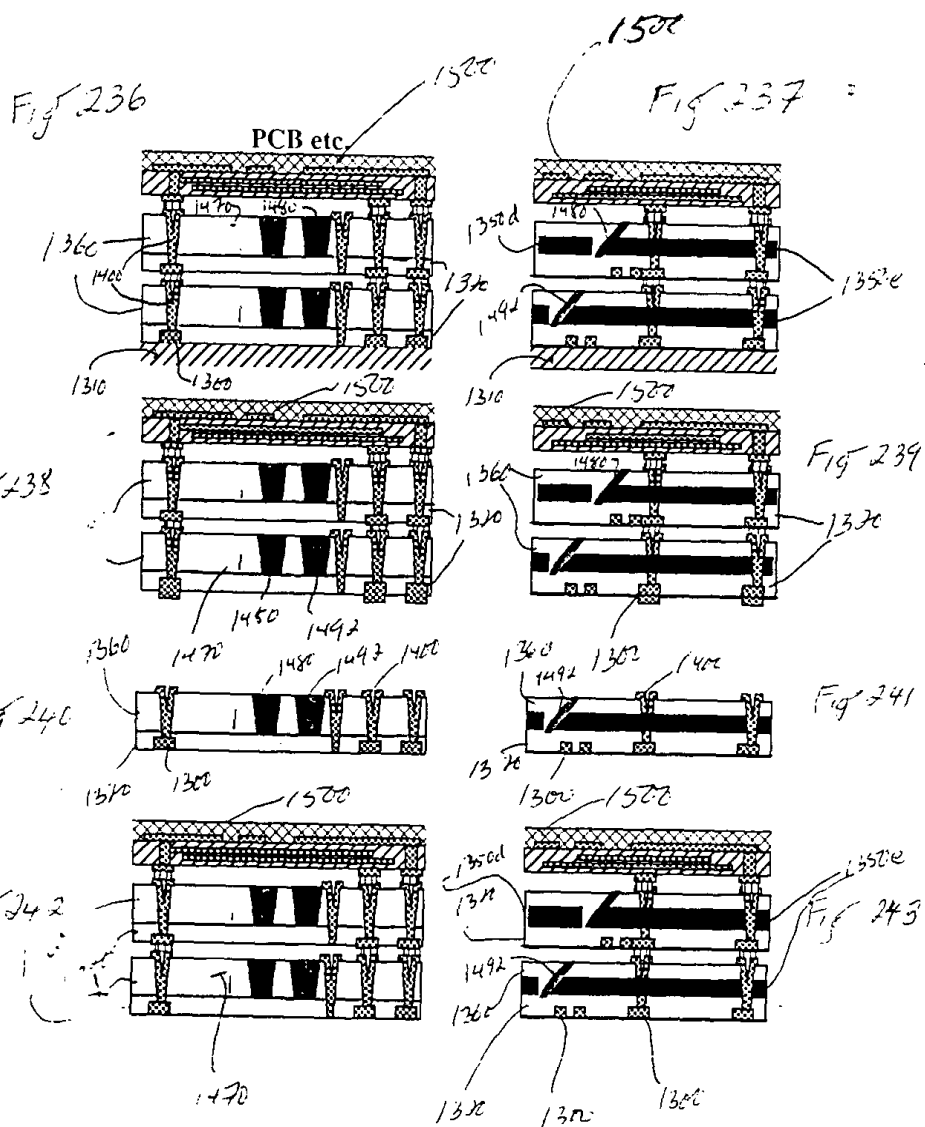


Fig 244

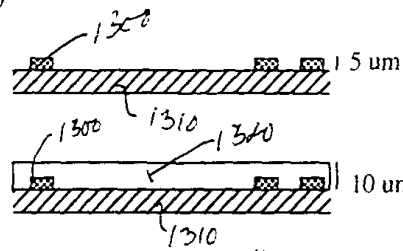


Fig 246

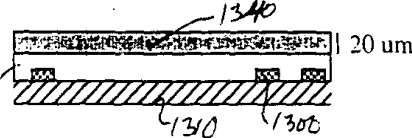


Fig 248

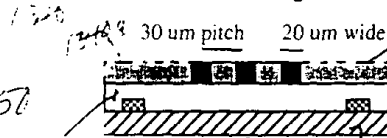


Fig 250

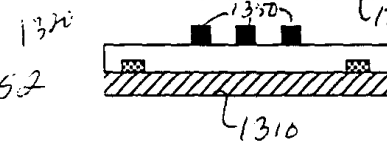


Fig 252

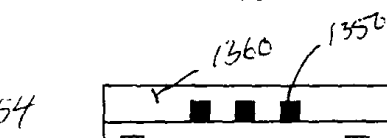


Fig 254

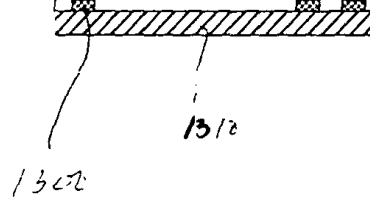


Fig 245

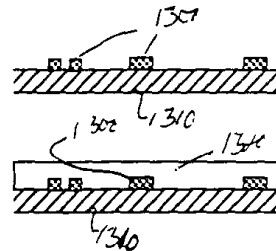


Fig 247

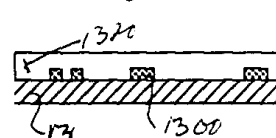


Fig 249

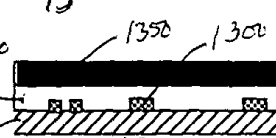


Fig 251

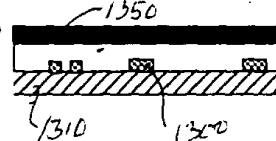


Fig 253

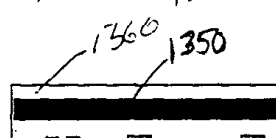
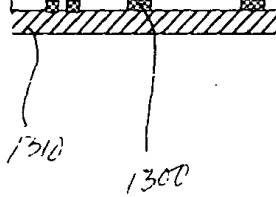
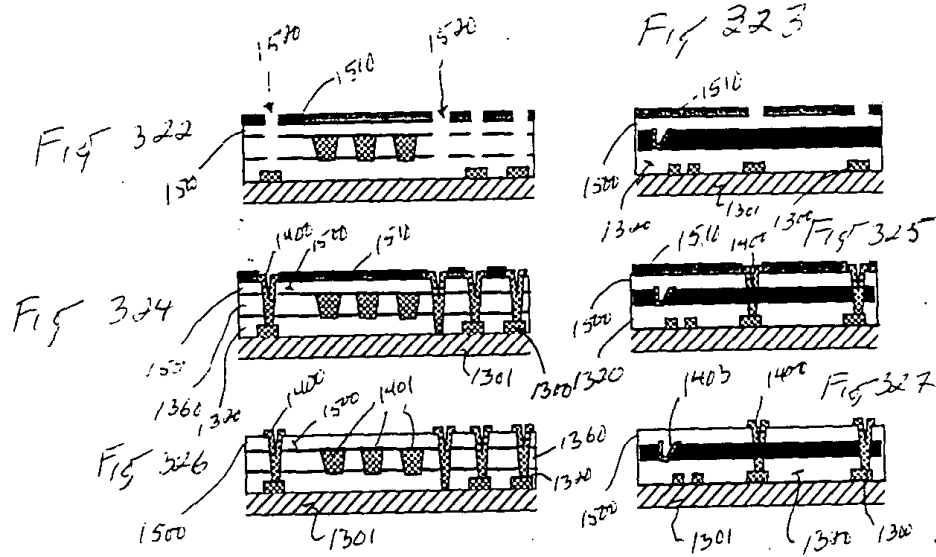


Fig 255







In the case of multi layer (a1-a12) process is repeated on the (a12).  
 -it is also possible to repeat (a3-a12) or (a1, a3-a12)

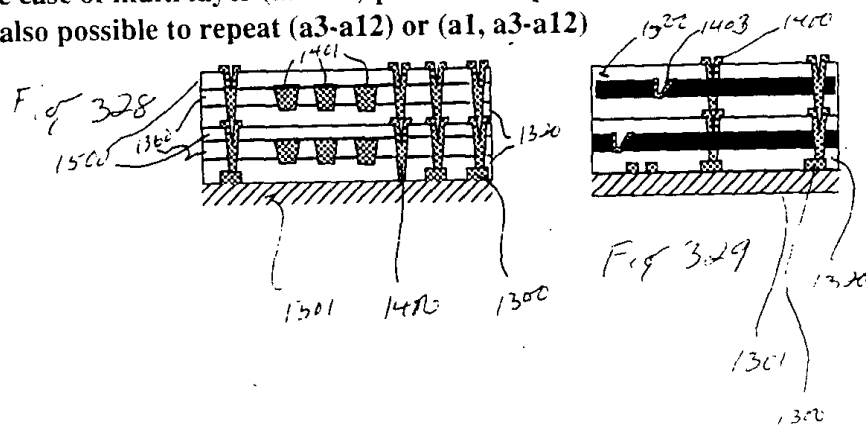
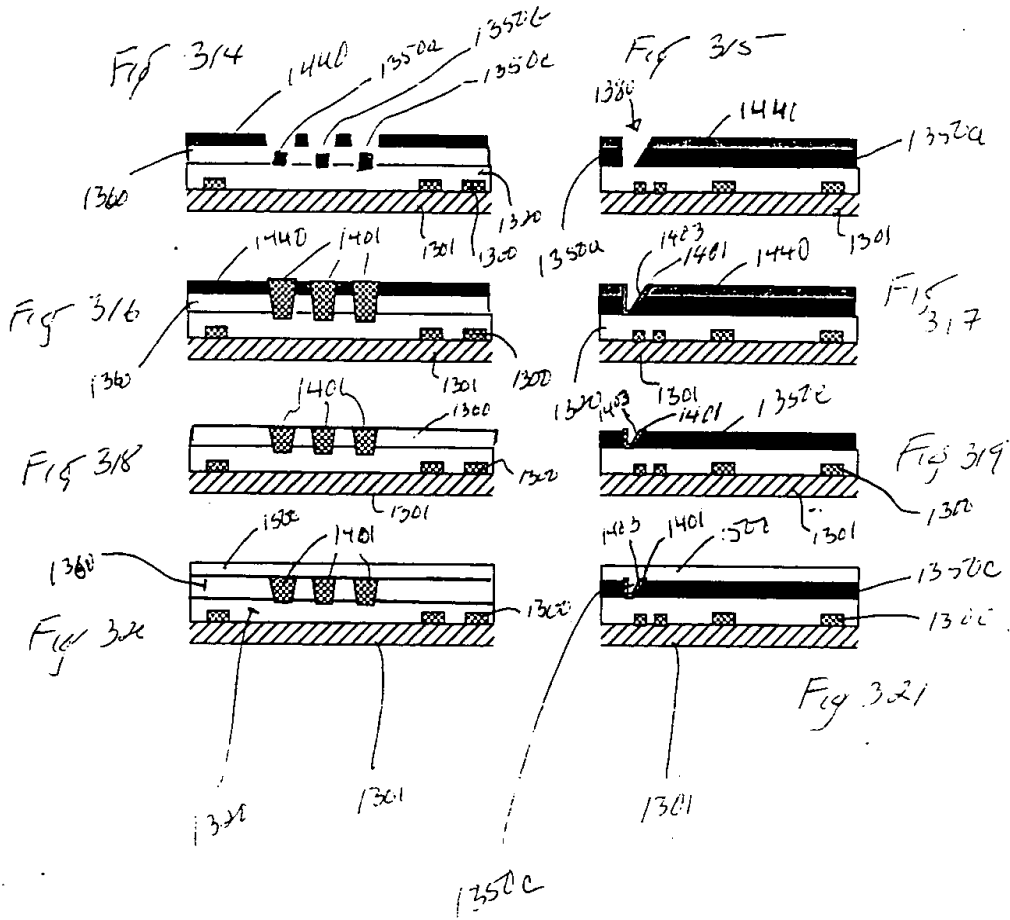


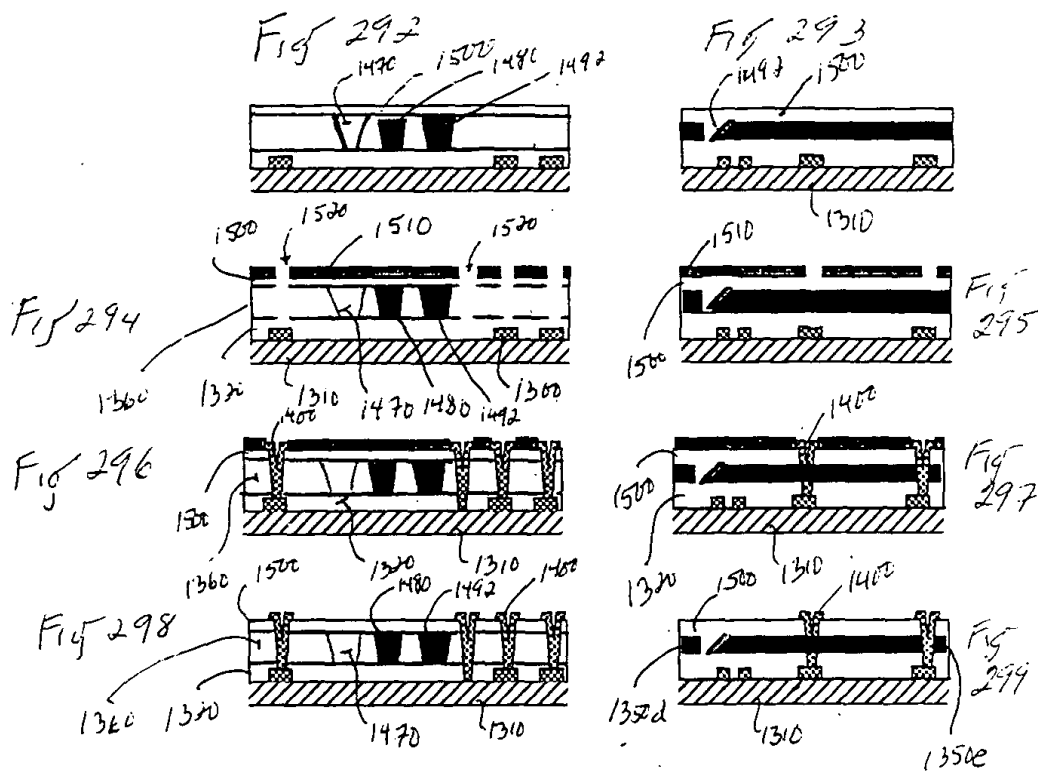
FIG. 3/14



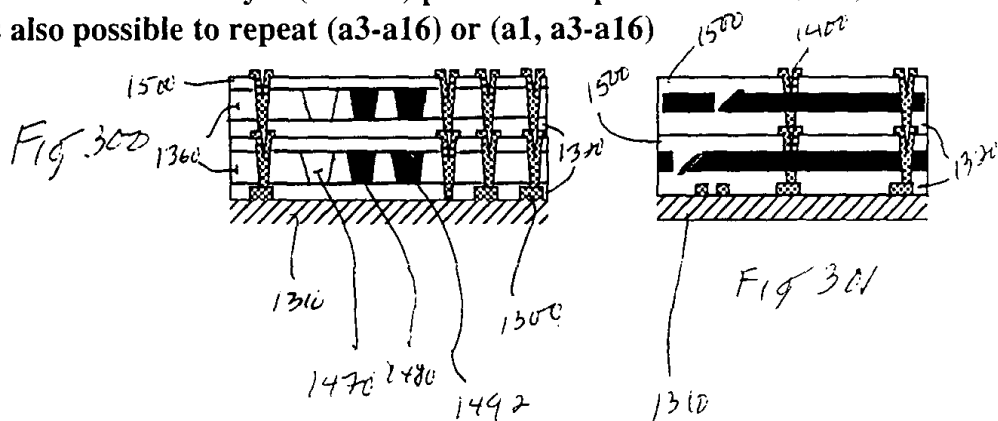








In the case of multi layer (a1-a16) process is repeated on the (a16).  
 -it is also possible to repeat (a3-a16) or (a1, a3-a16)



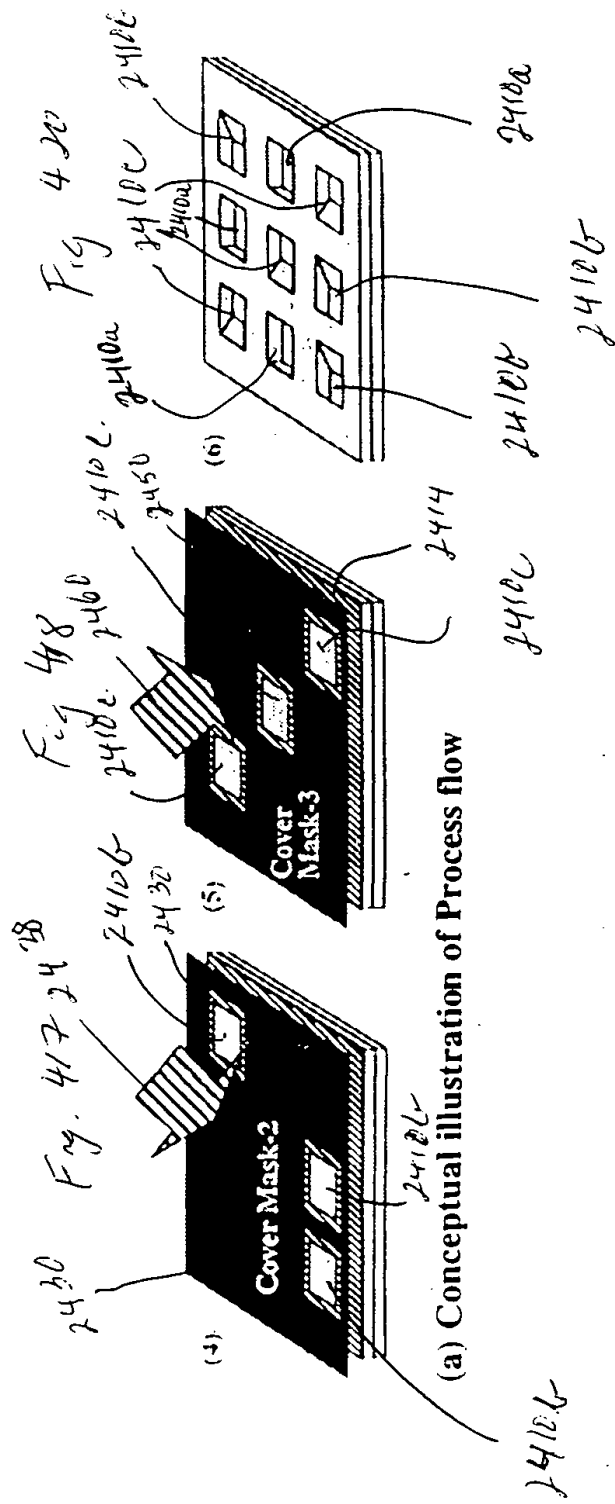
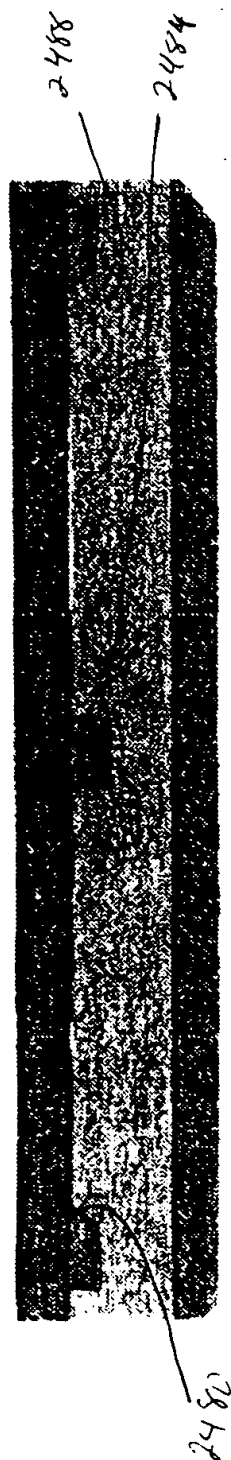


Fig. 4d1



250  $\mu\text{m}$

(b) Trench wall formation of three different angles